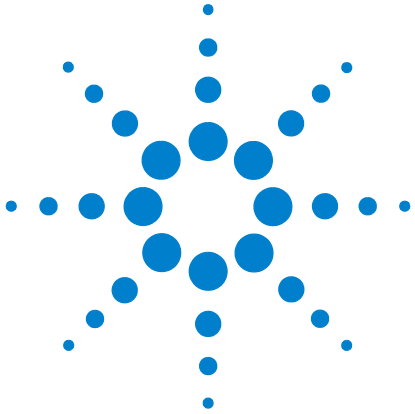

Agilent U7232A DisplayPort Electrical Performance Compliance Test Application

Compliance Testing Notes

Agilent Technologies

Notices

Manual Part Number

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DisplayPort Automated Testing—At A Glance

The Agilent U7232A DisplayPort Electrical Performance Compliance Test Application helps you verify DisplayPort Source device under test (DUT) compliance to DisplayPort specifications using an Agilent 8 GHz or greater Infiniium digital storage oscilloscope. The DisplayPort Electrical Performance Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the DisplayPort Electrical Performance Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Compliance testing measurements are described in Section 3, Source Compliance Tests, in the *DisplayPort- Compliance Test Specification Version 1* document. For more information, see the VESA web site at www.vesa.org.

Required Equipment and Software

In order to run the DisplayPort automated tests, you need the following equipment and software:

- 8 GHz or greater Infiniium Oscilloscope. Option 001 (1 M/ch memory upgrade) is recommended; this will greatly reduce Data Eye Pattern and Jitter test time.
- U7232A DisplayPort Electrical Performance Compliance Test Application.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable for calibrating the oscilloscope.
- E2655A/B probe de-skew fixture.

- 1168A or 1169A Probes
- Test fixture (W2641A). Includes four SMA to SMP cables.
- U7232A DisplayPort Electrical Performance Compliance Test Application license.
- N5400A EZJIT Plus Jitter Analysis software license (optional).

In This Book

This manual describes the tests that are performed by the DisplayPort Electrical Performance Compliance Test Application in more detail; it contains information from (and refers to) the *DisplayPort Specification Version 1*, and it describes how the tests are performed.

- Chapter 1, “Installing the DisplayPort Electrical Performance Compliance Test Application shows how to install and license the automated test application (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements shows how to start the DisplayPort Electrical Performance Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “Source Eye Diagram Testing shows the probing and test procedure of the data eye pattern tests.
- Chapter 4, “Source Total Jitter Tests contains more information on the source total jitter tests.
- Chapter 5, “Source Non-ISI Jitter Tests contains more information on the source non-isi jitter tests.
- Chapter 6, “Source Transition Time Tests describes the rise time and fall time tests.
- Chapter 7, “Source No Pre-emphasis Level Verification Testing describes the no pre-emphasis level verification tests.
- Chapter 8, “Source Pre-emphasis Level Verification Testing describes the pre-emphasis level verification tests.
- Chapter 9, “Source Frequency Accuracy Tests describes the source frequency accuracy tests.
- Chapter 10, “Source Inter-Pair Skew Tests describes the source inter-pair skew differential tests.
- Chapter 11, “Source Rise And Fall Time Mismatch Tests describes source intra-pair skew single-ended tests.
- Chapter 12, “Source Intra-Pair Skew Tests describes source intra-pair skew single-ended tests.
- Chapter 13, “Source AC Common Mode Noise Tests describes source AC common mode noise tests.
- Chapter 14, “Calibrating the Infiniium Oscilloscope and Probe describes how to calibrate the oscilloscope in preparation for running the DisplayPort automated tests.
- Chapter 15, “InfiniiMax Probing describes the 1168A/1169A probe amplifier and probe head recommendations for DisplayPort testing.

See Also

- The DisplayPort Electrical Performance Compliance Test Application's online help, which describes:
  - Creating or opening a test project.
  - Setting up the DisplayPort test environment.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running the tests.
  - Viewing the test results.
  - Viewing/printing the HTML test report.
  - Saving test projects.
  - Understanding the HTML report.

Contents

1 Installing the DisplayPort Electrical Performance Compliance Test Application

If you purchased the U7232A DisplayPort Electrical Performance Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1 Make sure you have version A.05.30 or higher of the Infiniium oscilloscope software by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the DisplayPort Electrical Performance Compliance Test Application, go to Agilent website: http://www.agilent.com/find/scope-apps-sw.

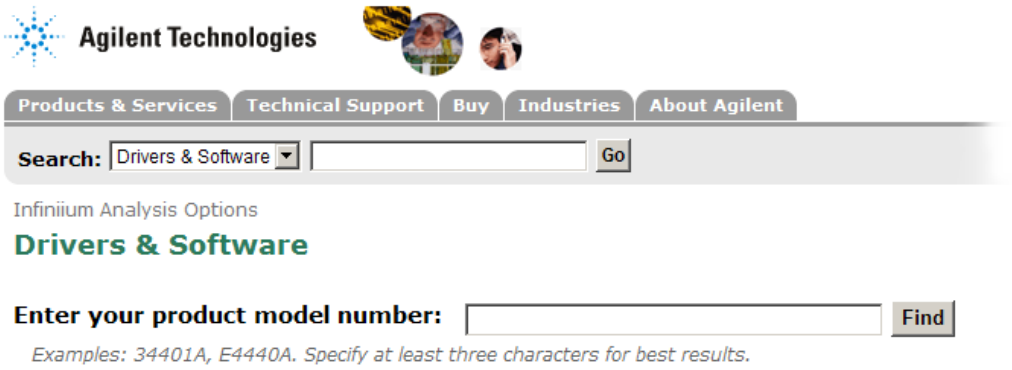

Figure 1 Agilent website for software Downloads

3 Search the list on this web page for the link to the U7232A DisplayPort Electrical Performance Compliance Test Application. Click on it and follow the instructions to download and install the application.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application to complete the license installation.

1 Installing the DisplayPort Electrical Performance Compliance Test Application

2 Preparing to Take Measurements

Before running the DisplayPort automated tests, you need to acquire the appropriate test fixtures, and you should calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the DisplayPort Electrical Performance Compliance Test Application and perform the measurements.

W2641A Test Fixture

The W2641A test fixture is the Agilent DisplayPort test fixture that is used for all of the DisplayPort compliance tests.

Acquiring the Test Fixture

The W2641A DisplayPort test fixture can be acquired from Agilent Technologies.

W2641A Test Fixture Description

Figure 2 shows the top view of the W2641A test fixture.

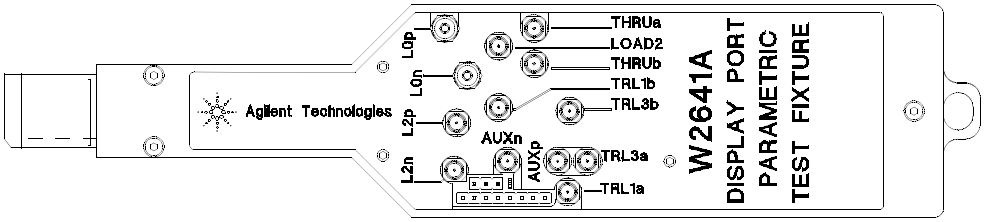

Figure 2 W2641A DisplayPort Test Fixture (Top View)

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 14, "Calibrating the Infiniium Oscilloscope and Probe.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DisplayPort Electrical Performance Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>DisplayPort Test**.

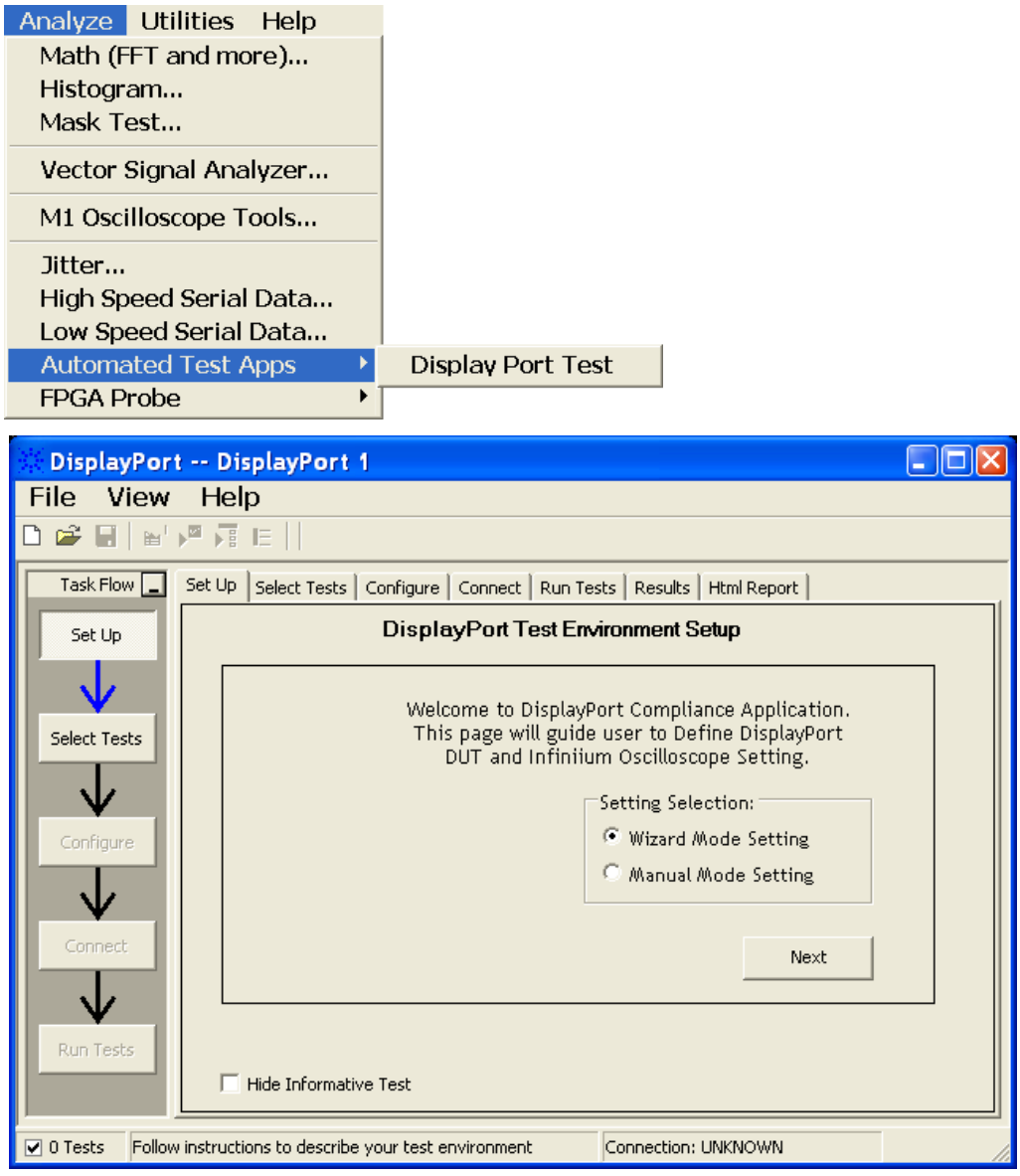

Figure 3 The DisplayPort Electrical Performance Compliance Test Application

NOTE If DisplayPort Test does not appear in the Automated Test Apps menu, the DisplayPort Electrical Performance Compliance Test Application has not been installed (see Chapter 1, "Installing the DisplayPort Electrical Performance Compliance Test Application).

Figure 3 shows the DisplayPort Electrical Performance Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you select your setup options. Allows you to setup by connection type, device identifier, jitter separation measurements and test fixture type.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically, so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you enter information about the device being tested and configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE When you close the DisplayPort application, each channel's probe is configured as single-ended or differential depending on the last DisplayPort test that was run.

Online Help Topics

For information on using the DisplayPort Electrical Performance Compliance Test Application, see the online help (which you can access by choosing **Help>Contents**... from the application's main menu).

The DisplayPort Electrical Performance Compliance Test Application's online help describes:

- Starting the DisplayPort Electrical Performance Compliance Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Running the Compliance Test Application on a second monitor.
- Creating or opening a test project.
- Setting up DisplayPort test environment.
- Selecting the tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running the tests.
- Viewing test results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
  - To change report trial display.
- Viewing or printing the HTML test report.
- Saving the test projects.
- Understanding the DisplayPort HTML report.

3 Source Eye Diagram Testing

This section provides the guidelines for source data eye pattern differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

NOTE Agilent Option 001 (1M/ch memory upgrade) is recommended; this will greatly reduce Data Eye Pattern test time.

Probing for Differential Tests

When performing the data eye pattern test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 4 below: two Connection by using W2641A Test Fixture, then your physical connection for the data eye test should be similar to Figure 5.

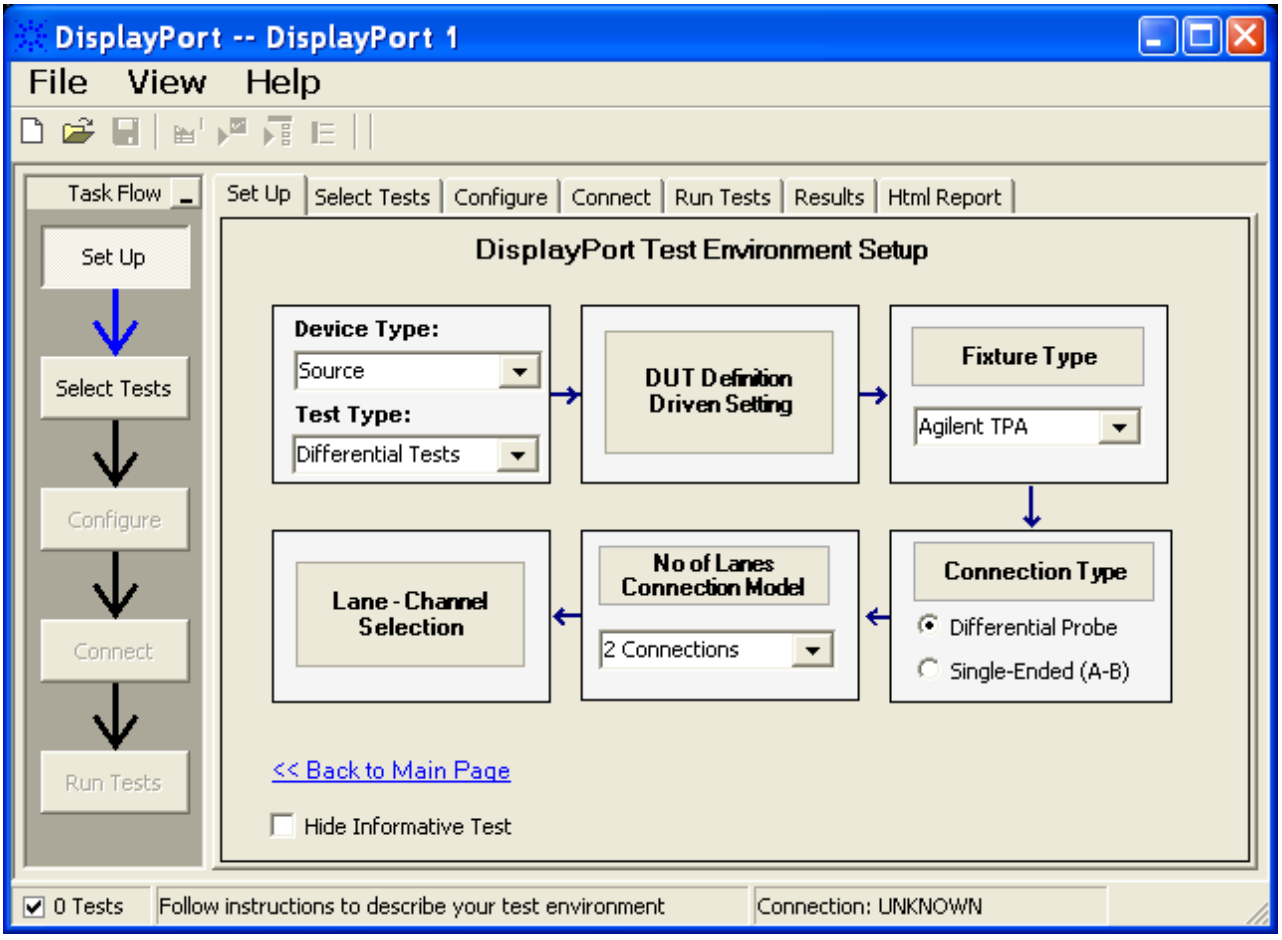

Figure 4 Setup for Data Eye Pattern Differential Tests (Two Connections with W2641A DisplayPort Test Fixture)

Figure 6 shows a physical connection for making single-ended connections.

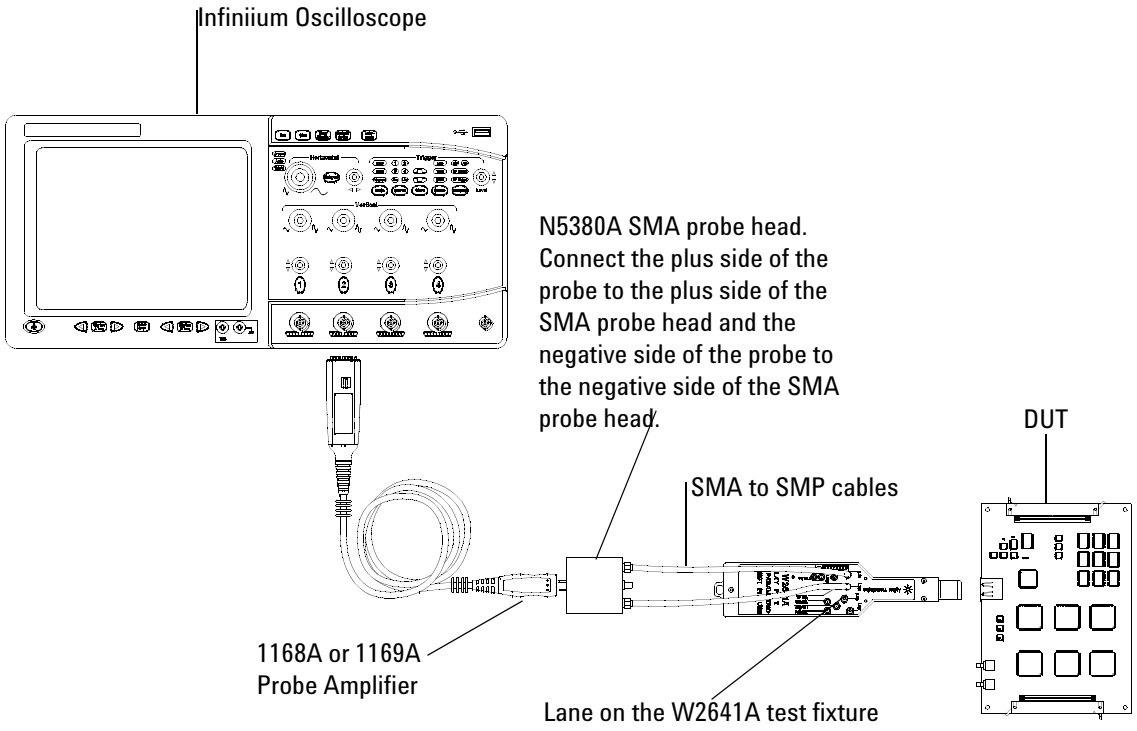

Figure 5 Probing for Differential Tests - Data Eye Pattern Tests using the W2641A DisplayPort Test Fixture)

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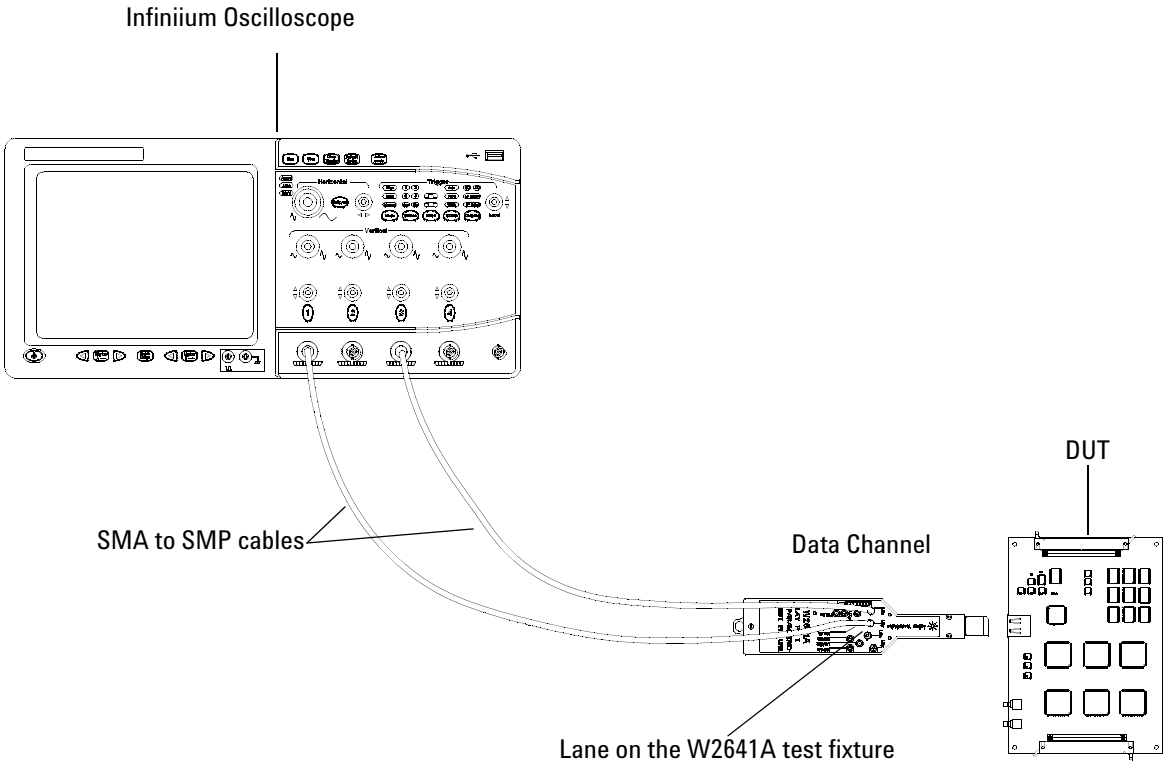

Figure 6 Probing for Single-ended Tests - Data Eye Pattern Tests using the W2641A DisplayPort Test Fixture

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 147.

Source Eye Diagram Test

The eye diagram test provides a visual evaluation of the amplitude and timing variations of the waveform with the overall objective of obtaining a specified Bit Error Rate in transmitted data. The test must use a PRBS7 test pattern at all voltage levels. The test should be performed without pre-emphasis.

The source Eye Diagram performance provides the best visual assessment of interoperability potential by showing amplitude and timing minimums and maximum values.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the Eye Diagram - Lane # - Eye Diagram Test where # is the lane number to be tested.

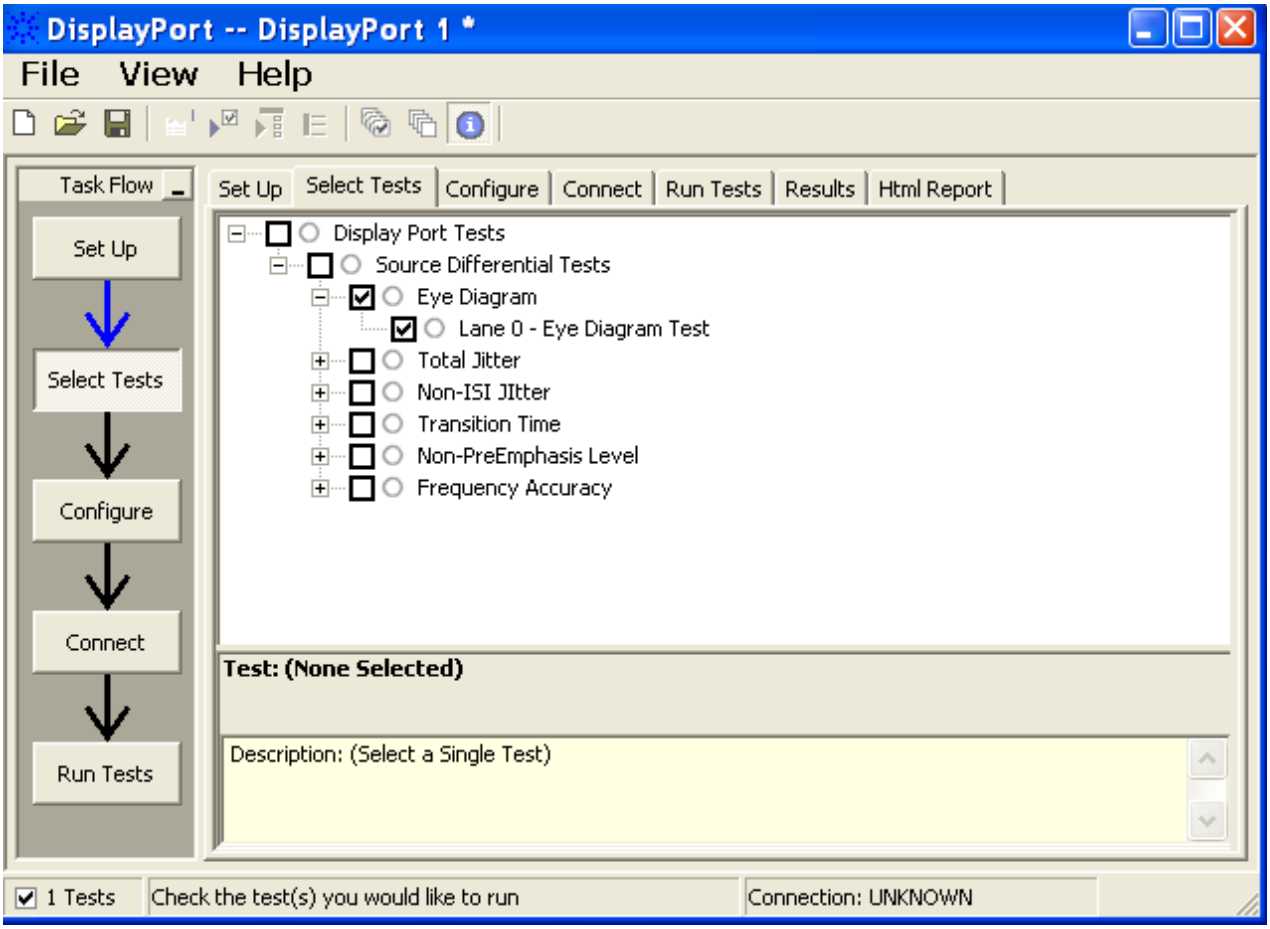

Figure 7 Selecting Data Eye Pattern Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 1), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 1 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.

Table 1 Test Configuration Options

Configuration Option	Description
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.

Table 1 Test Configuration Options

Configuration Option	Description
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 2 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 2 Eye Diagram Mask Coordinates

	Bit Rate	
Mask Point	**Reduced (1.6 Gb/s)**	**High (2.7 Gb/s)**
1	0.102, 0.000	0.159, 0.000
2	0.277, 0.255	0.332, 0.158
3	0.500, 0.318	0.500, 0.198
4	0.723, 0.318	0.668, 0.198
5	0.899, 0.000	0.844, 0.000
6	0.723,-0.318	0.665,-0.198
7	0.500,-0.318	0.500,-0.198
8	0.277,-0.255	0.332,-0.158

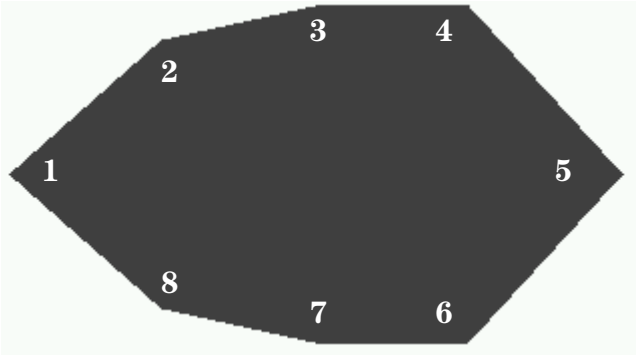

Figure 8 The Source Eye Pattern Mask

Mask Test: Zero mask failures.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort- Compliance Test Specification Version 1.*

4 Source Total Jitter Tests

This section provides the guidelines for source total jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

NOTE Agilent Option 001 (1M/ch memory upgrade) is recommended; this will greatly reduce Jitter test time.

Probing for Total Jitter Test

When performing the total jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 9 below: two Connection by using W2641A Test Fixture, then your physical connection for the data eye test should be similar to Figure 10.

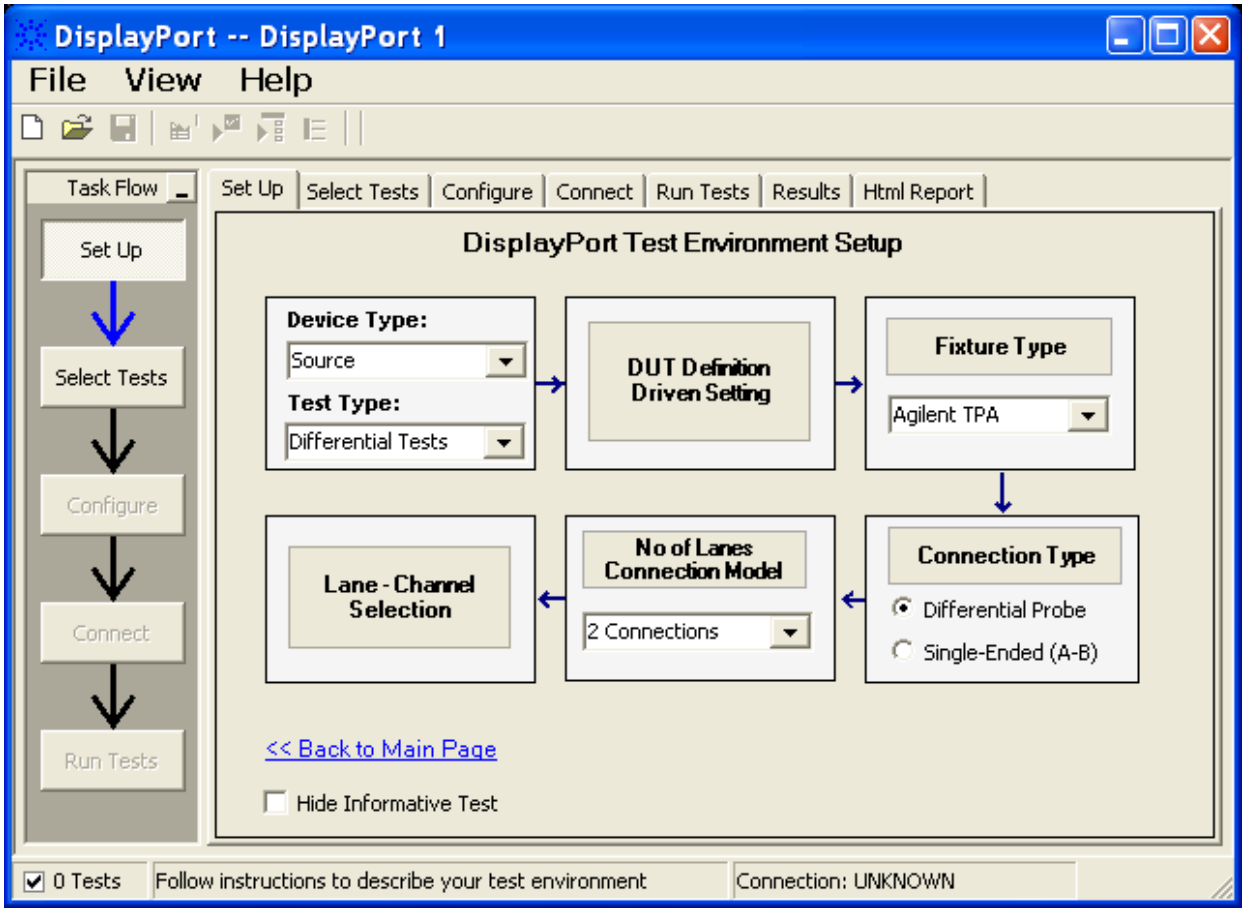

Figure 9 Setup for Total Jitter Test (1 Connection with W2641A DisplayPort Parametric Test Fixture)

Figure 10 and Figure 11 below show the single-ended and differential connections for the Total Jitter Tests.

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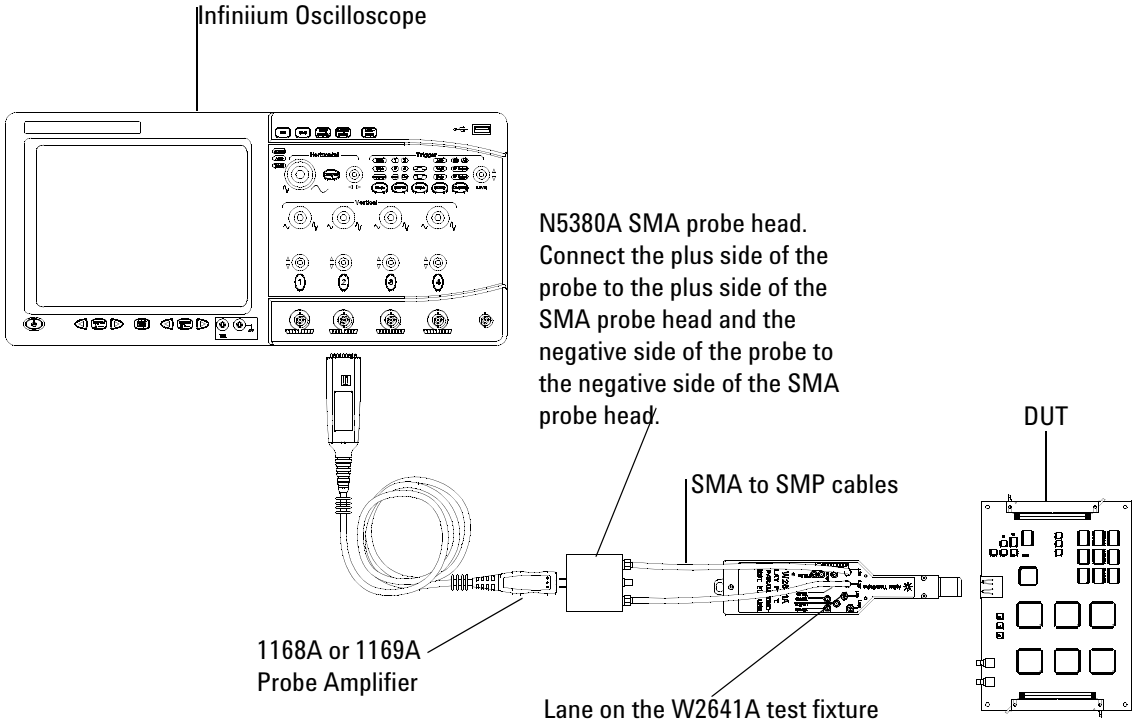

Figure 10 Probing for Differential Tests - Total Jitter Tests (Two Connections with W2641A DisplayPort Test Fixture)

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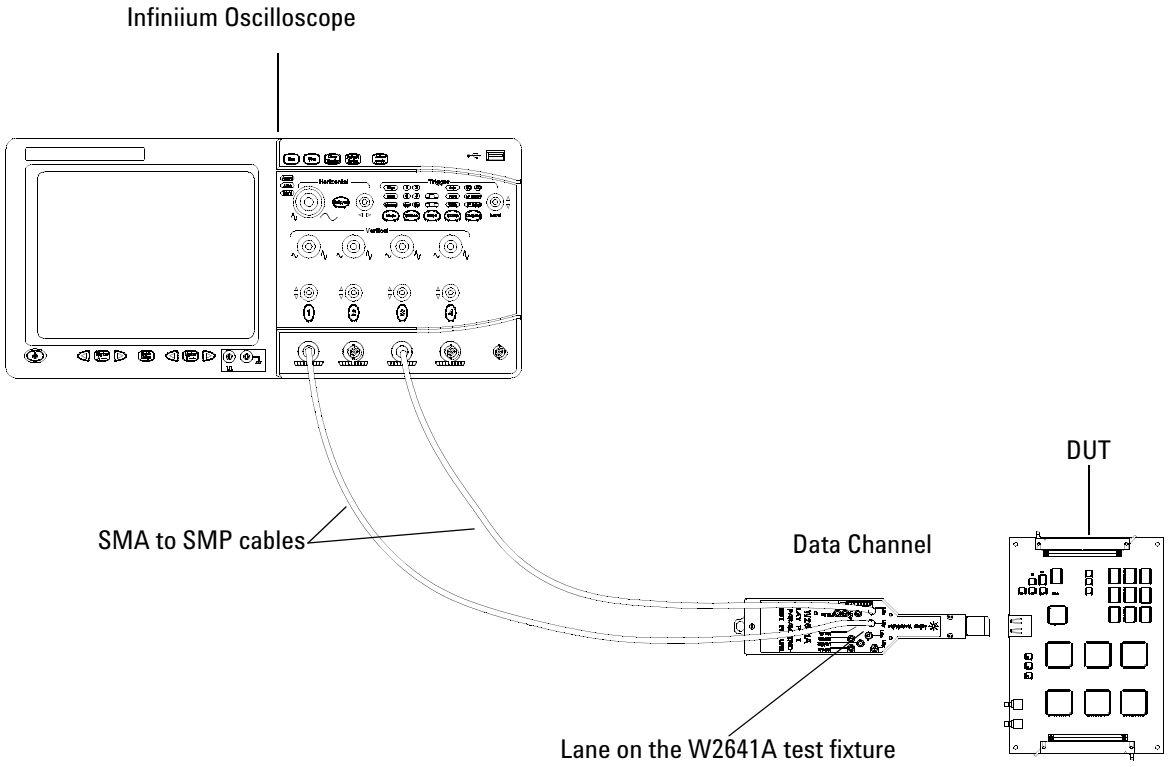

Figure 11 Probing for Single-ended Tests - Total Jitter Tests using the W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Total Jitter Differential Test

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference: Table 3.13 VESA DisplayPort Standard)

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)

The test must use a PRBS7 test pattern at all voltage levels. The test can be performed with pre-emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the Total Jitter - Lane # - where # is the lane number to be tested.

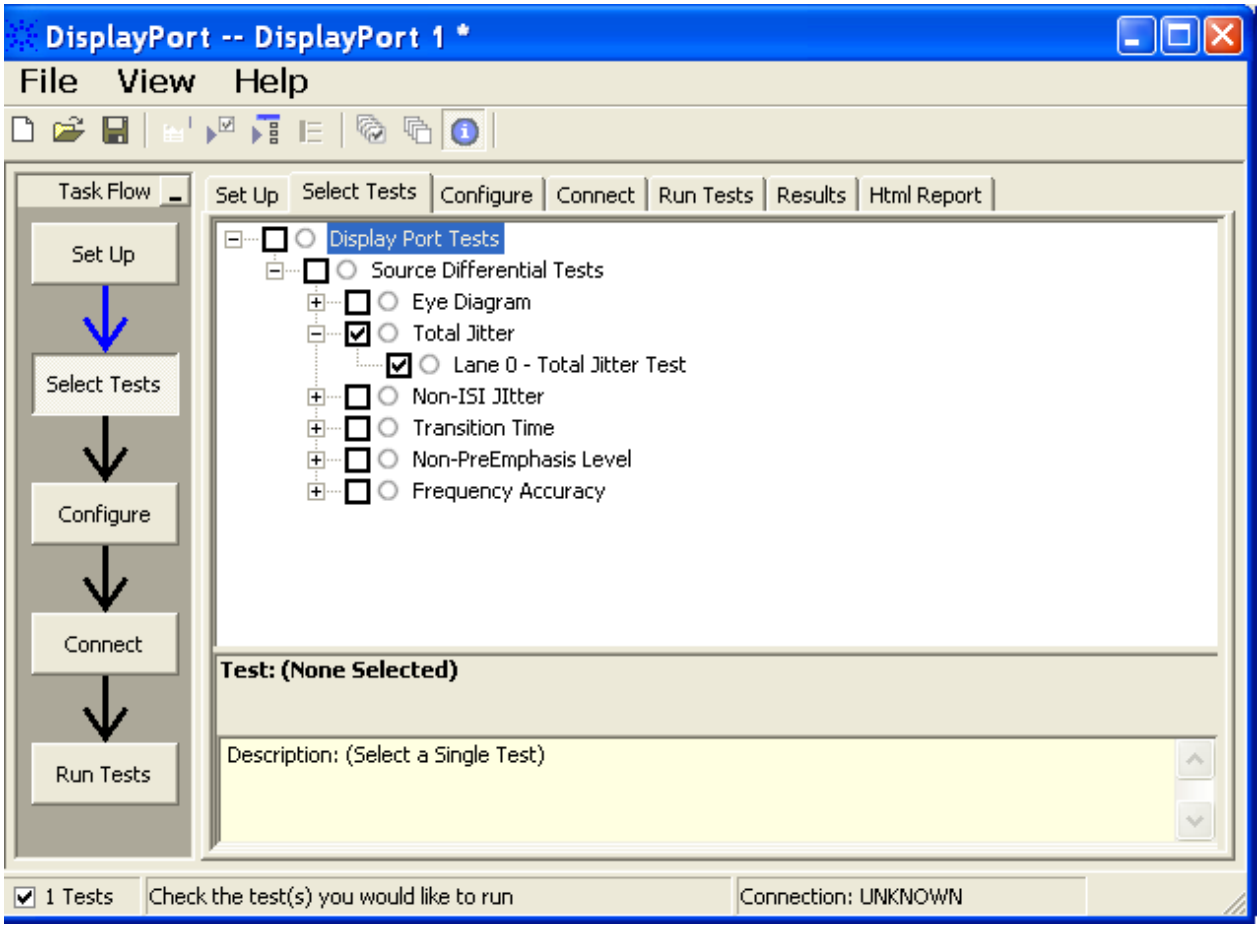

Figure 12 Selecting Total Jitter Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 3), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 3 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 3 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 3 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

Table 4 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.364 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.223 UI

UI is Unit Interval.

Test References

See Test 3.12: Total Jitter (TJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1.*

4 Source Total Jitter Tests

5 Source Non-ISI Jitter Tests

This section provides the guidelines for source non-ISI jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

NOTE Agilent Option 001 (1M/ch memory upgrade) is recommended; this will greatly reduce Jitter test time.

Probing for Non-ISI Jitter Test

When performing the non-ISI jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 13: one Connection using the W2641A DisplayPort Parametric Test Fixture, 1168A or 1169A differential probe with N5380A SMA probe head then your physical connection for the jitter test should be similar to Figure 14.

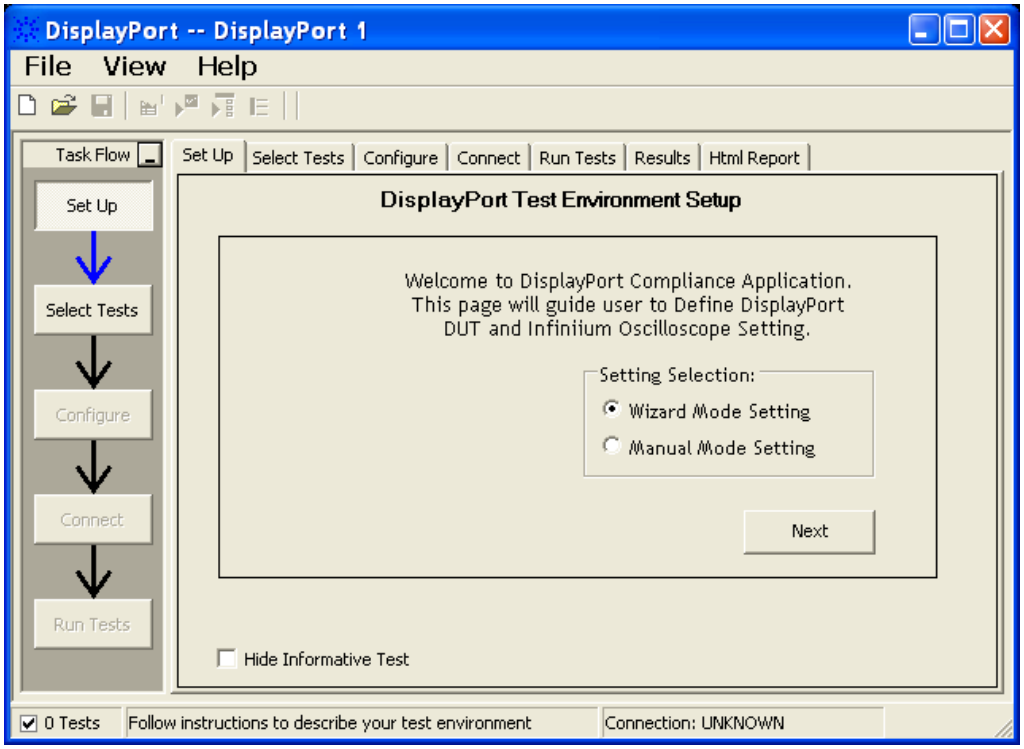

Figure 13 Setup for Non-ISI Jitter Test (1 Connection with W2641A DisplayPort Parametric Test Fixture)

Figure 14 and Figure 15 below show the single-ended and differential connections for Non-ISI Jitter Tests.

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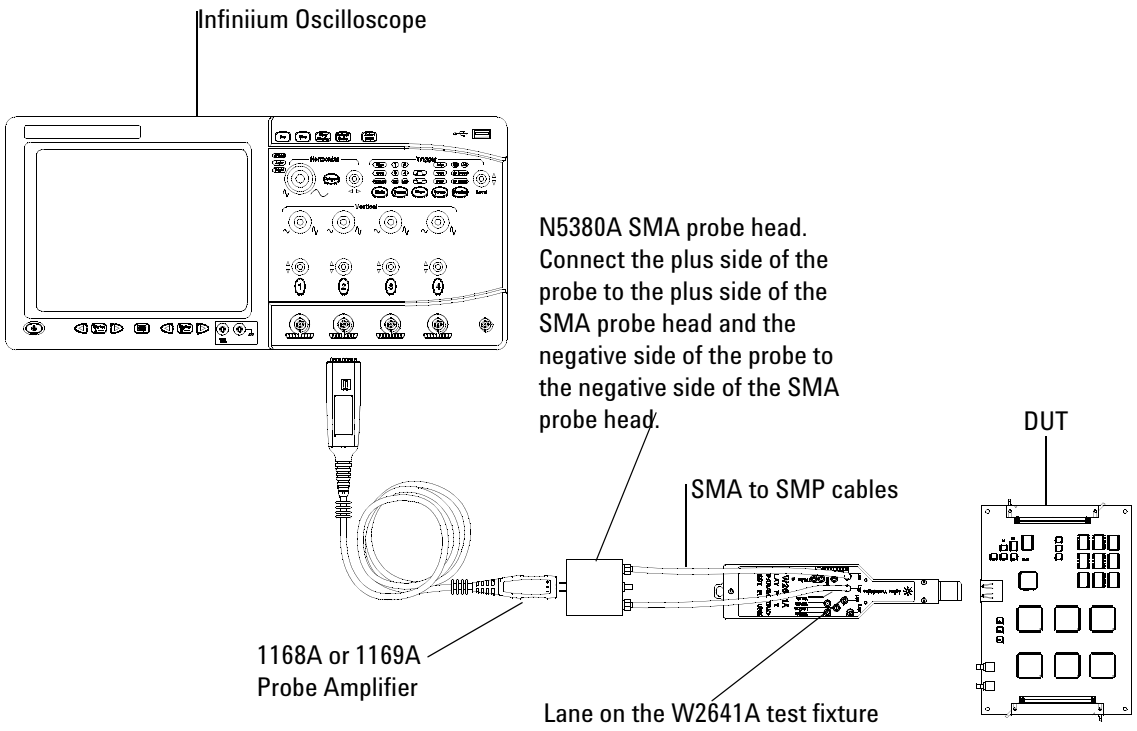

Figure 14 Probing for Differential Tests - Non-ISI Jitter Tests (Two Connections with W2641A DisplayPort Test Fixture)

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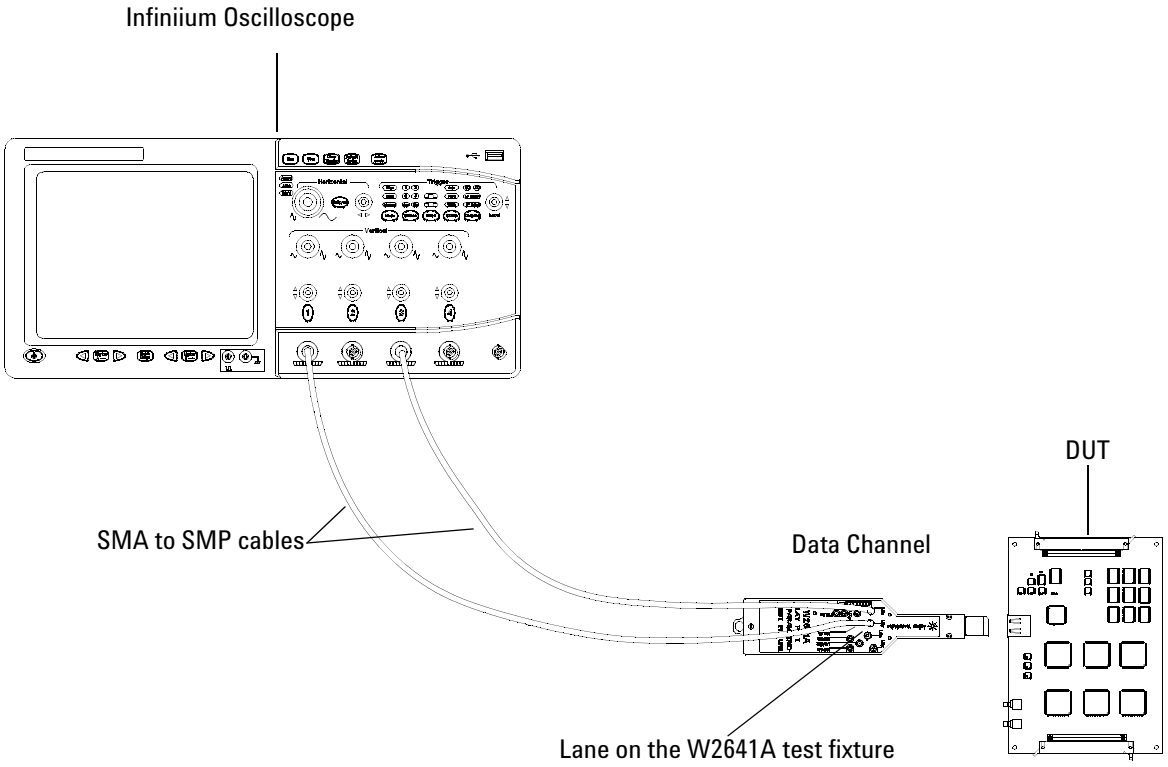

Figure 15 Probing for Single-ended Tests - Non-ISI Jitter Tests (Four Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Non-ISI Jitter Test

To evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. (Reference: Table 3.13 VESA DisplayPort Standard)

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)

The test must use a PRBS7 test pattern at all voltage levels. The test can be performed with pre-emphasis for best performance results.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the Non-ISI Jitter - Lane # - Non-ISI Jitter Test where # is the lane number to be tested.

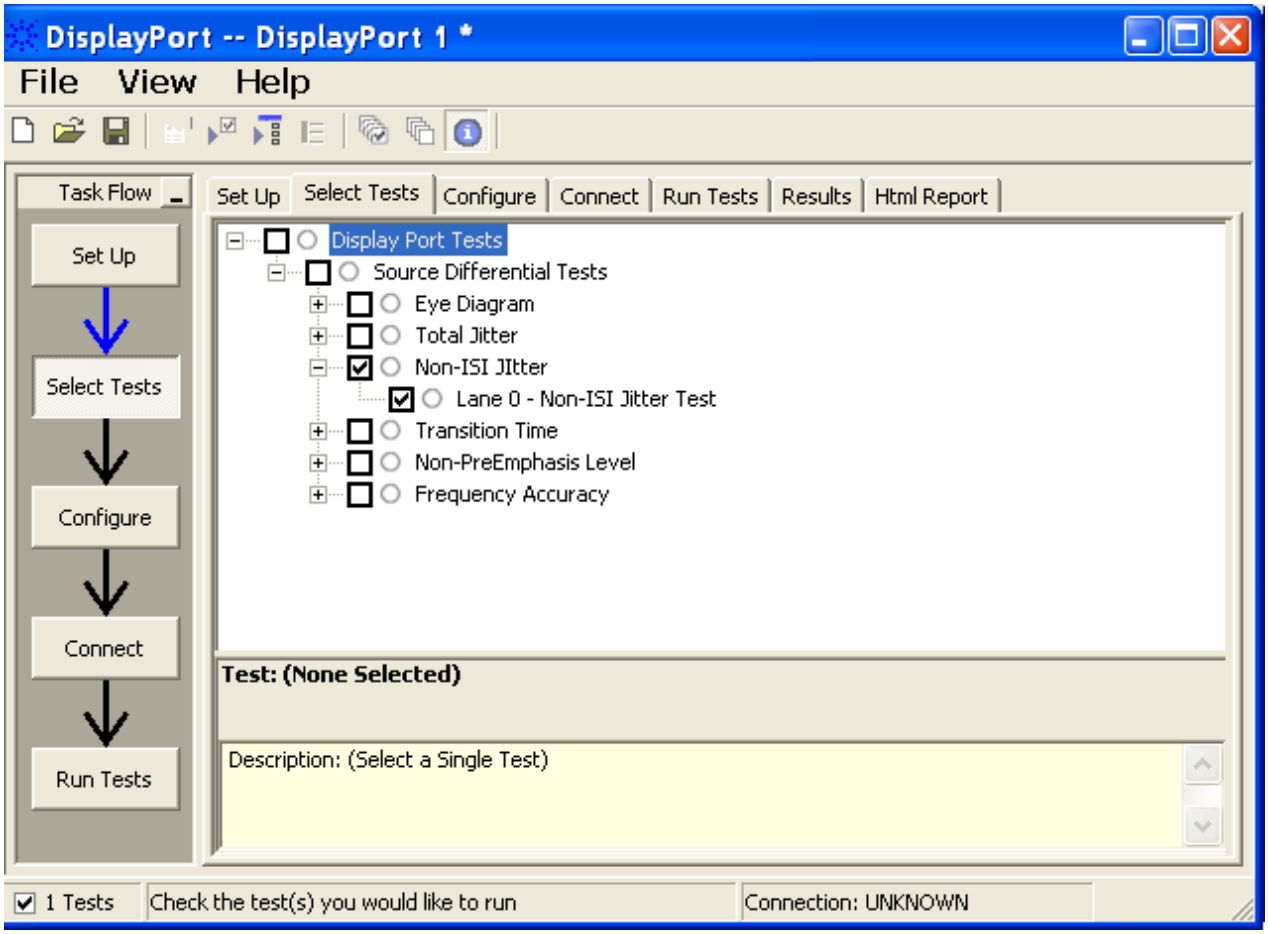

Figure 16 Selecting Data Eye Pattern Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 5), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 5 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL; ζ = the dampling factor of the PLL; F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 5 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 5 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

Table 6 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.364 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.223 UI

UI is Unit Interval.

Test References

See Test 3.12: Non-ISI Jitter (TJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1.*

6 Source Transition Time Tests

This section provides the guidelines for source transition time tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Transition Time Tests

When performing the transition time test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 17 below: two Connection by using W2641A Test Fixture, then your physical connection for the transition time test should be similar to Figure 18.

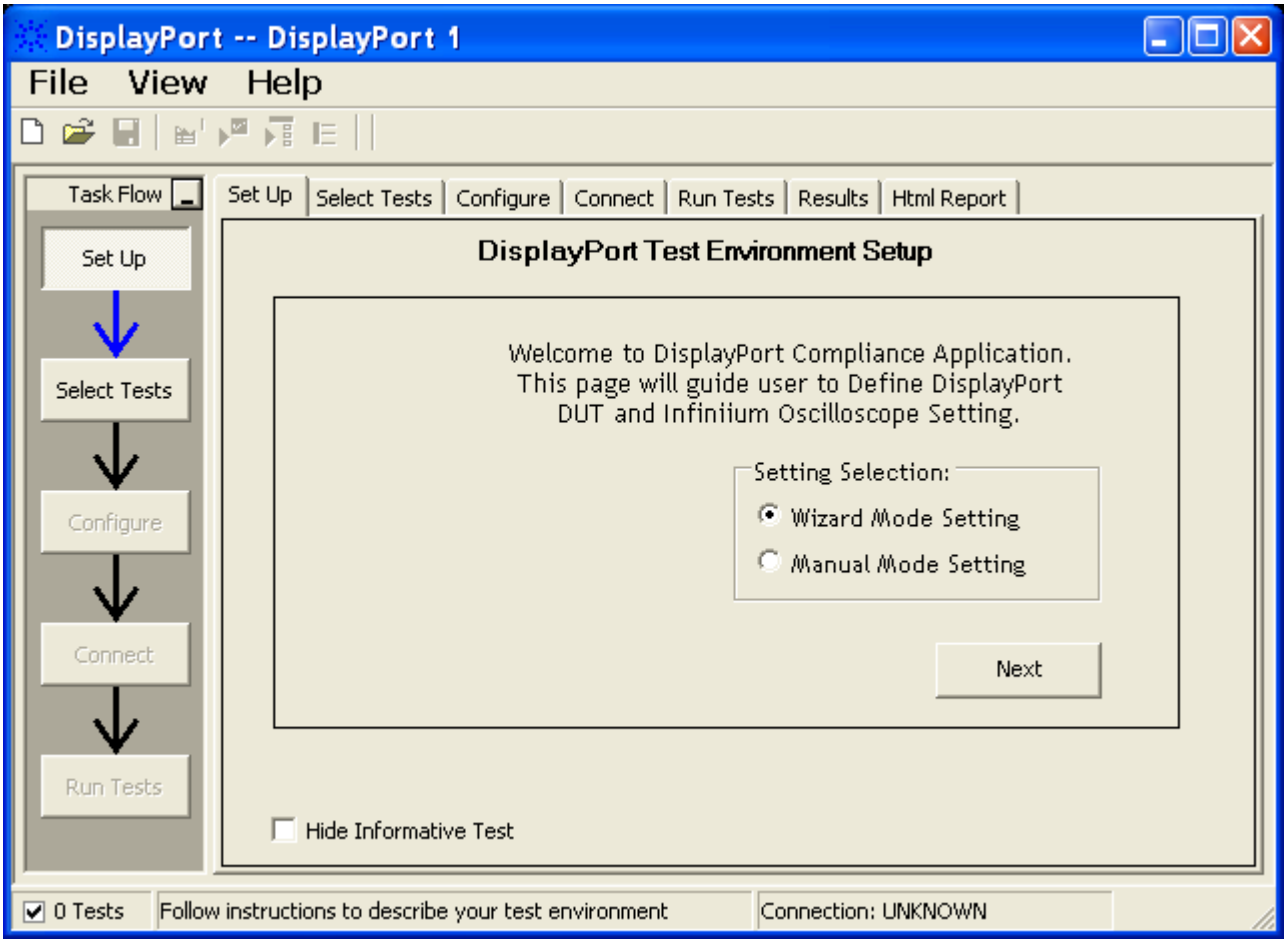

Figure 17 Setup for Transition Time Differential Tests (Two Connections with W2641A DisplayPort Test Fixture)

Figure 18 and Figure 19 below show the single-ended and differential connections for Transition Time Tests.

.

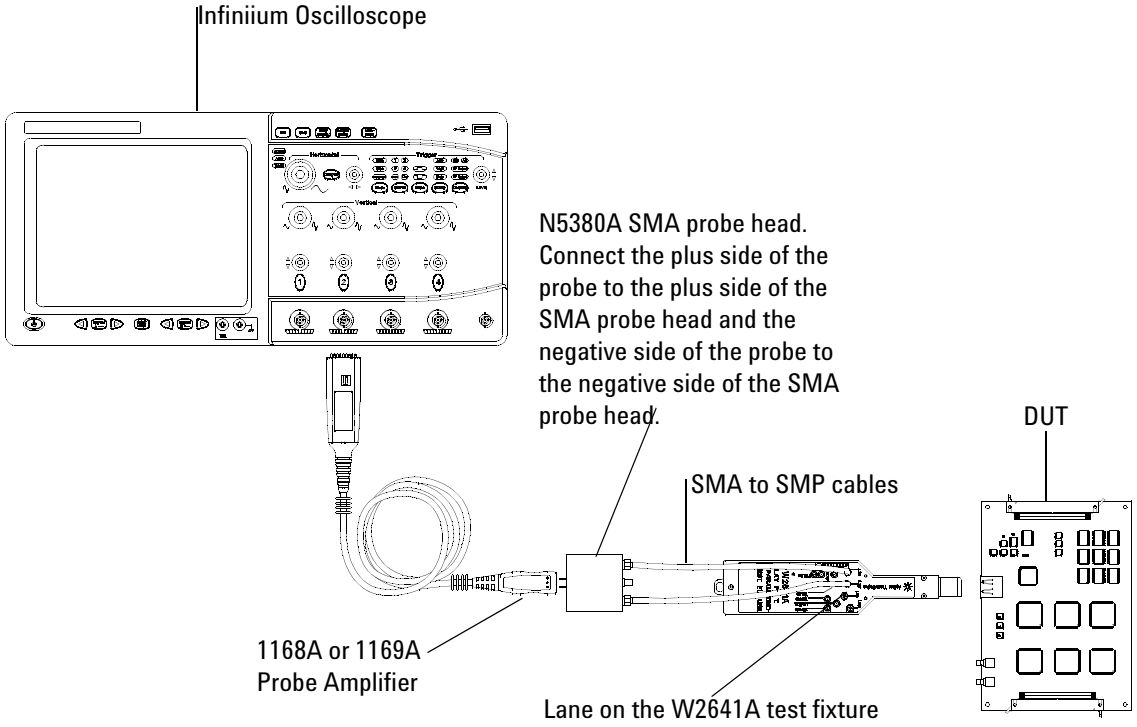

Figure 18 Probing for Differential Tests - Transition Time Tests (Two Connections with W2641A DisplayPort Test Fixture)

.

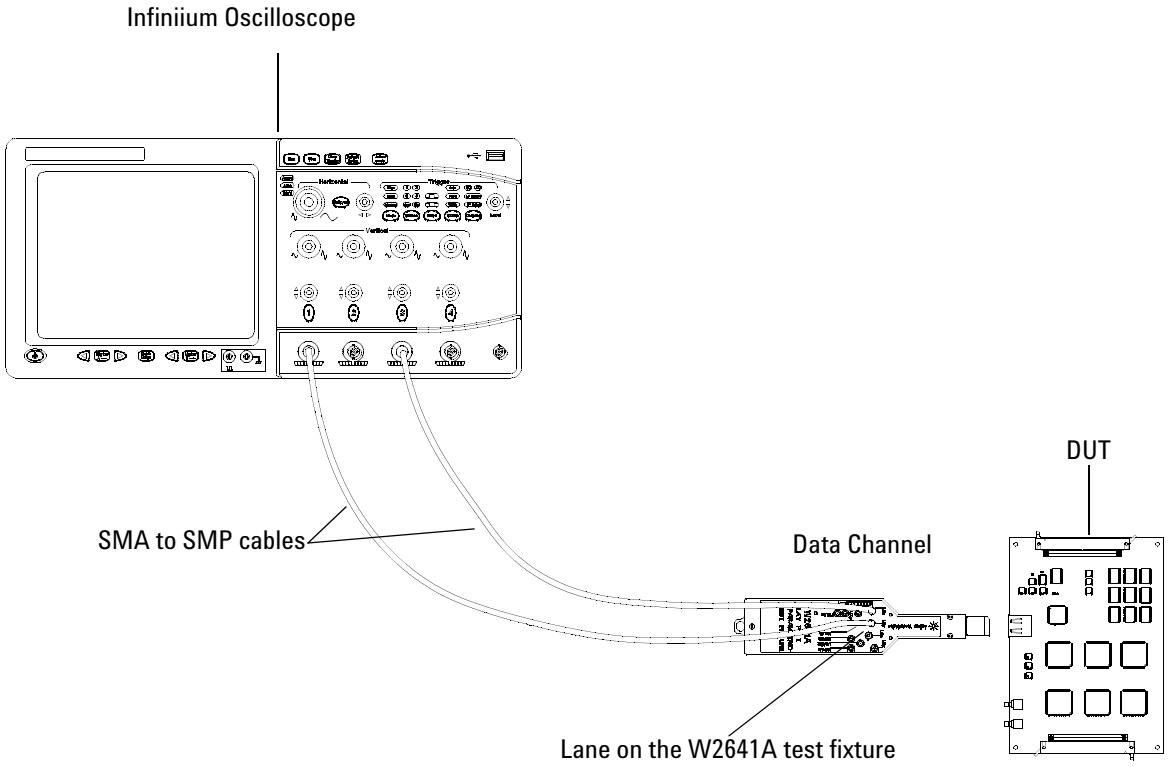

Figure 19 Probing for Single-ended Tests - Transition Time Tests (Four Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Transition Time Differential Tests

Transition time testing measures the rise time and fall time across the outputs of a differential data lane. The transition is defined as the time interval between the normalized 20% and 80% amplitude levels.

The transition time test should be performed at all bit rates supported without pre-emphasis for 400 mV differential voltage swing. The source pattern should be a PRBS7 waveform. This applies to one, two, and four lane operation with all functional lanes being tested. (Reference: Table 3.10 VESA DisplayPort Standard)

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the Transition Time group, and check the rise time and fall time tests that you want to perform.

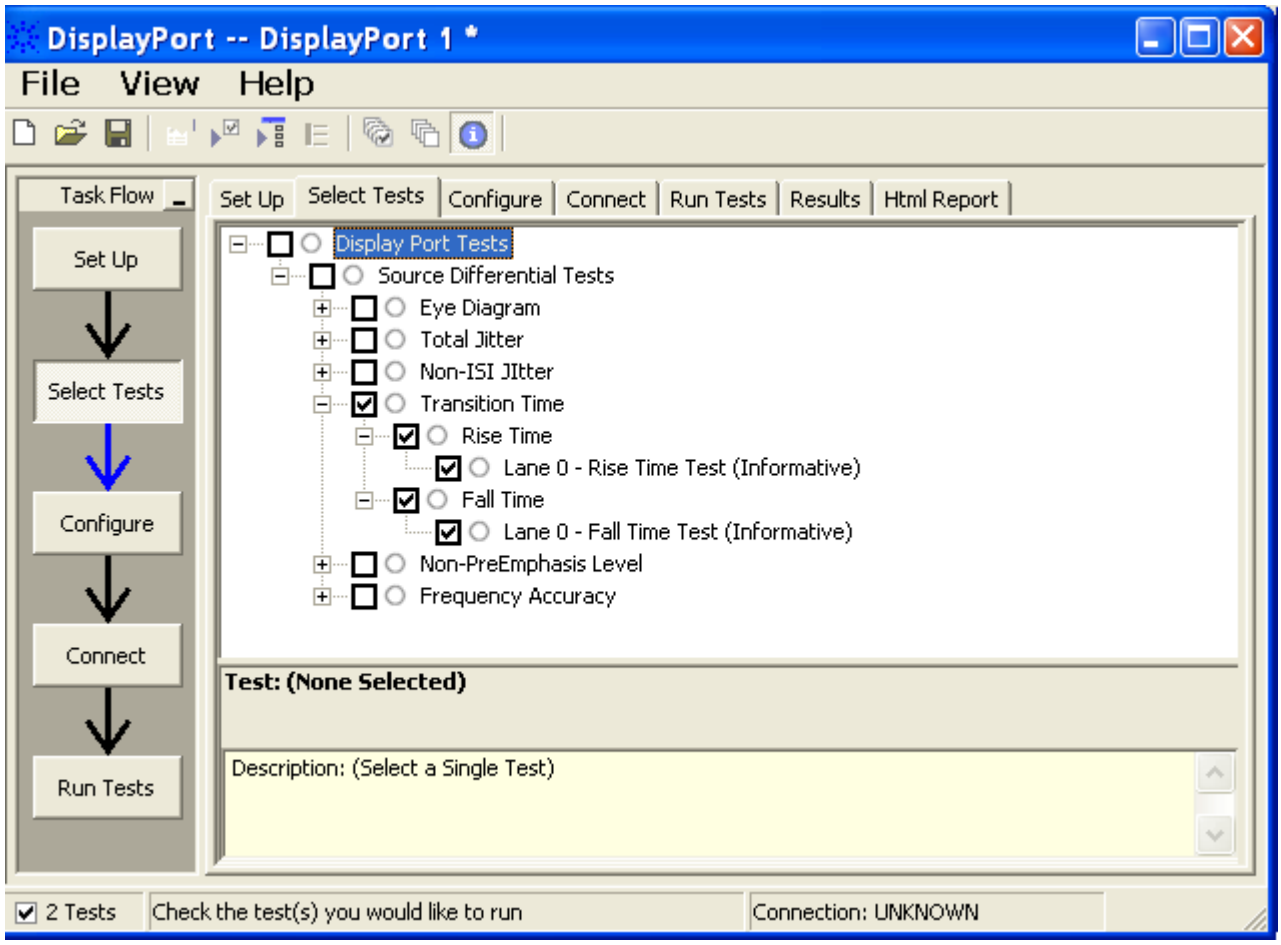

Figure 20 Selecting Transition Time Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 7), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 7 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL; ζ = the dampling factor of the PLL; F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 7 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 7 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

50 ps ≤ Transition Time ≤ 160 ps

Test References

See section 3.6, in the *DisplayPort- Compliance Test Specification Version 1*.

7 Source No Pre-emphasis Level Verification Testing

This section provides the guidelines for source no pre-emphasis level verification testing using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for No Pre-emphasis Level Verification Testing

When performing the no pre-emphasis level verification test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 21 below: two Connection by using W2641A Test Fixture, then your physical connection for the no pre-emphasis level verification test should be similar to Figure 22.

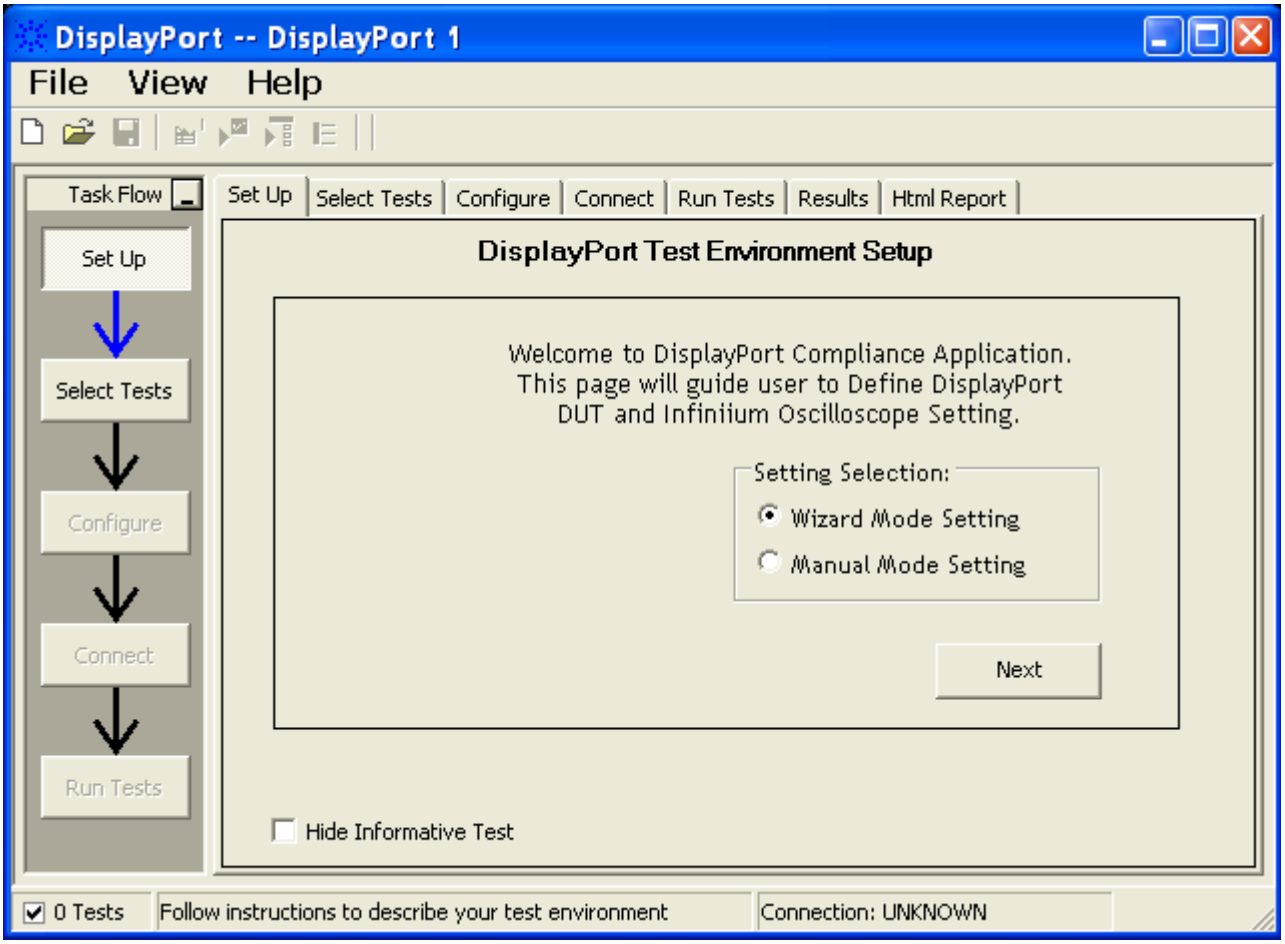

Figure 21 Setup for no pre-emphasis level verification Differential Tests (Two Connections with W2641A DisplayPort Test Fixture)

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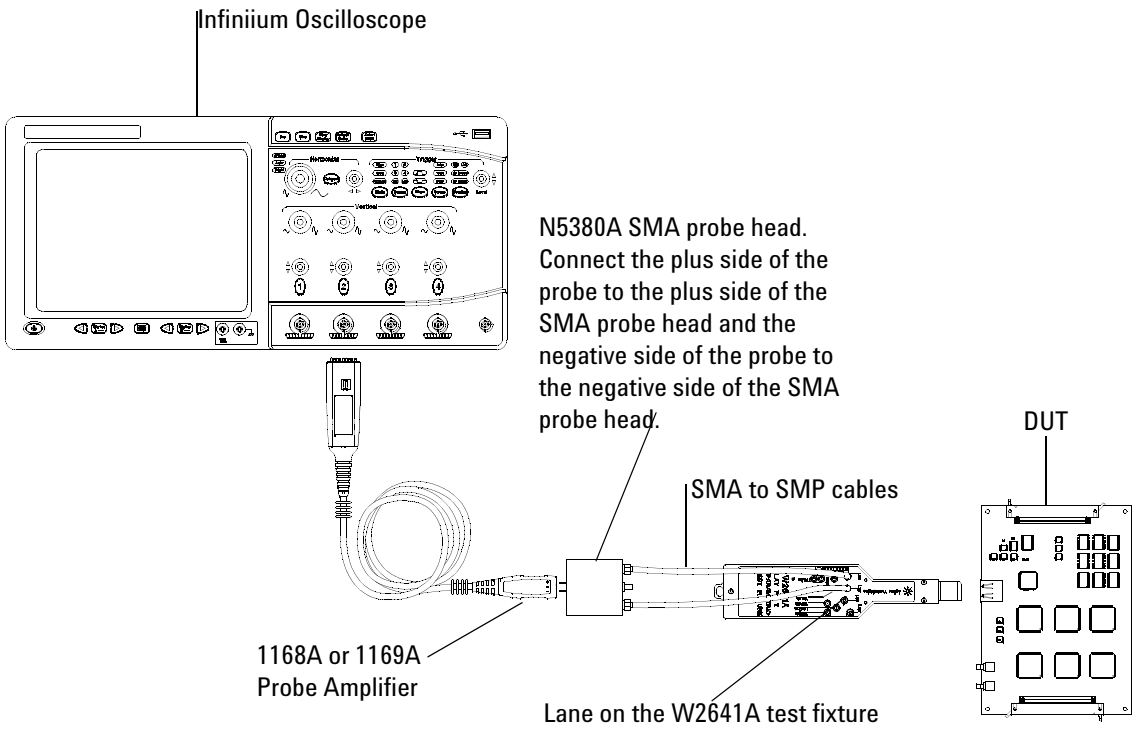

Figure 22 Probing for Differential Tests - No Pre-emphasis Level Verification Tests (Two Connections with W2641A DisplayPort Test Fixture)

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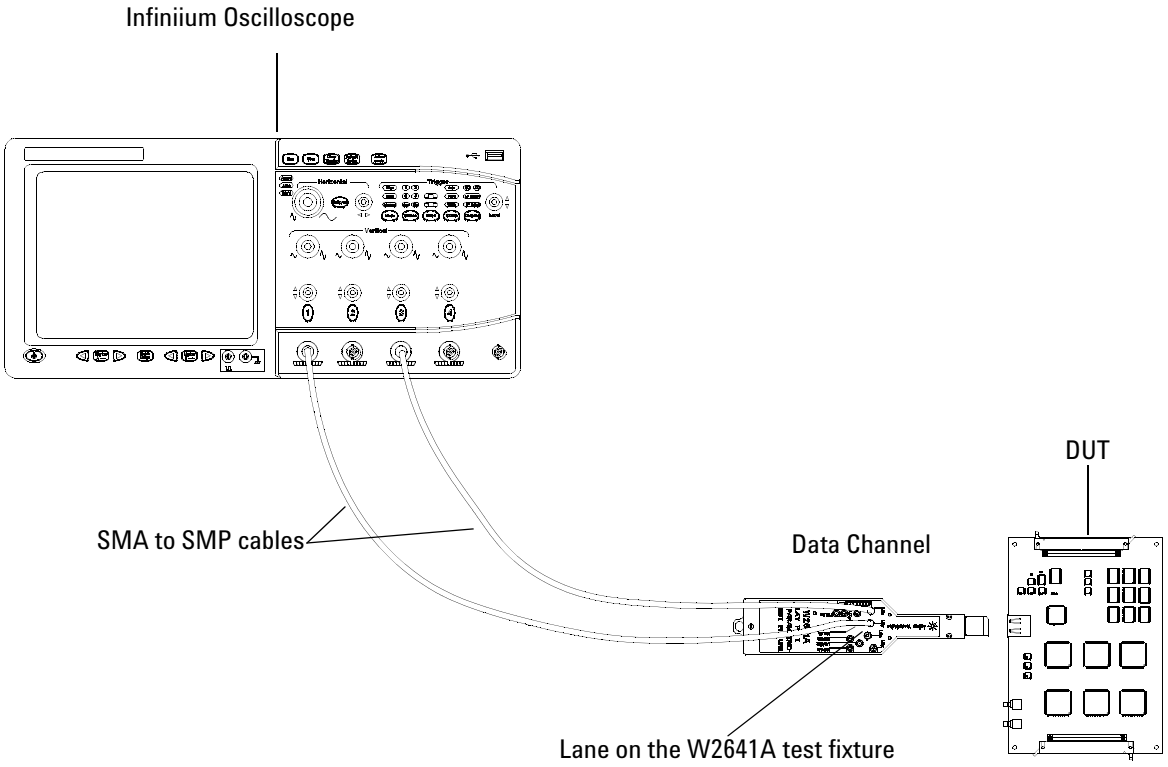

Figure 23 Probing for Single-ended Tests - No Pre-emphasis Level Verification Tests (Two Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

No Pre-emphasis Level Verification Test

To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven. (Reference: Table 3.10 VESA DisplayPort Standard)

The source is given a range of expected output for each level setting that correlates with the system budget elements such as cable loss and receiver eye minimum and max values. This test ensures that the system budget is obeyed.

The amplitude measurement is performed using the following equation at all bit rates without pre-emphasis and a PRBS 7 waveform:

$$\text{Peak-to-peak Voltage} = V_H - V_L$$

where:

V_H is the high voltage level
V_L is the low voltage level

Test Procedure

1. Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

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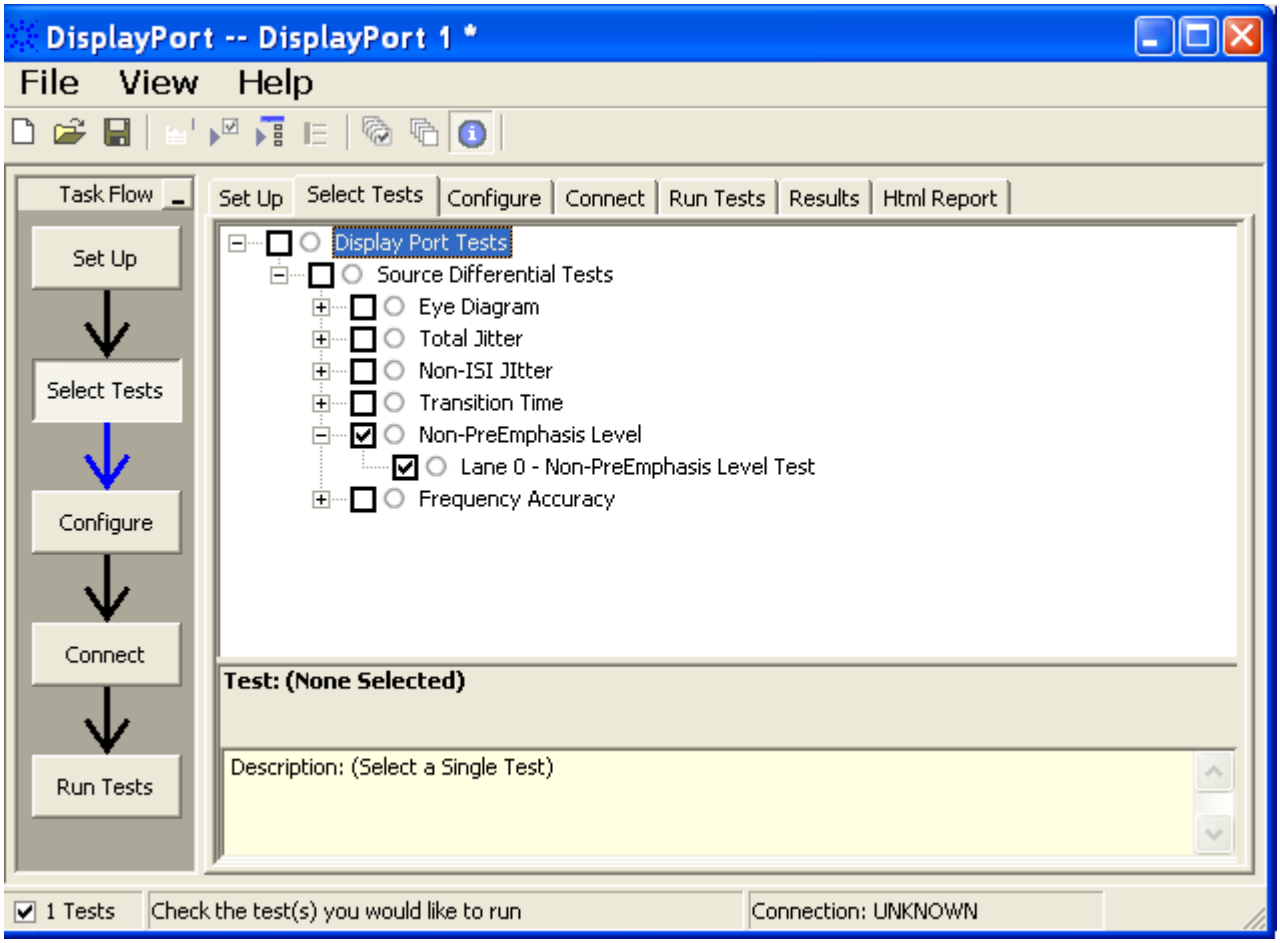

Figure 24 Selecting No Pre-emphasis Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 8), make oscilloscope connections, run the tests, and view the test results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 8 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL; ζ = the dampling factor of the PLL; F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 8 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 8 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

The peak-to-peak voltage must fall within the following ranges for each output level:

Output level 1 (0.4 V): 0.34 V ≤ Result ≤ 0.46 V

Output level 2 (0.6 V): 0.51 V ≤ Result ≤ 0.68 V

Output level 3 (0.8 V): 0.69 V ≤ Result ≤ 0.92 V

Output level 4 (1.2 V): 1.02 V ≤ Result ≤ 1.38 V

Test References

See Test 3-2: No Pre-emphasis Level Verification Testing, in the *DisplayPort-Compliance Test Specification Version 1.*

7 Source No Pre-emphasis Level Verification Testing

8 Source Pre-emphasis Level Verification Testing

This section provides the guidelines for source pre-emphasis level verification testing using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Pre-emphasis Level Verification Testing

When performing the pre-emphasis level verification test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 25 below: two Connection by using W2641A Test Fixture, then your physical connection for the pre-emphasis level verification test should be similar to Figure 26.

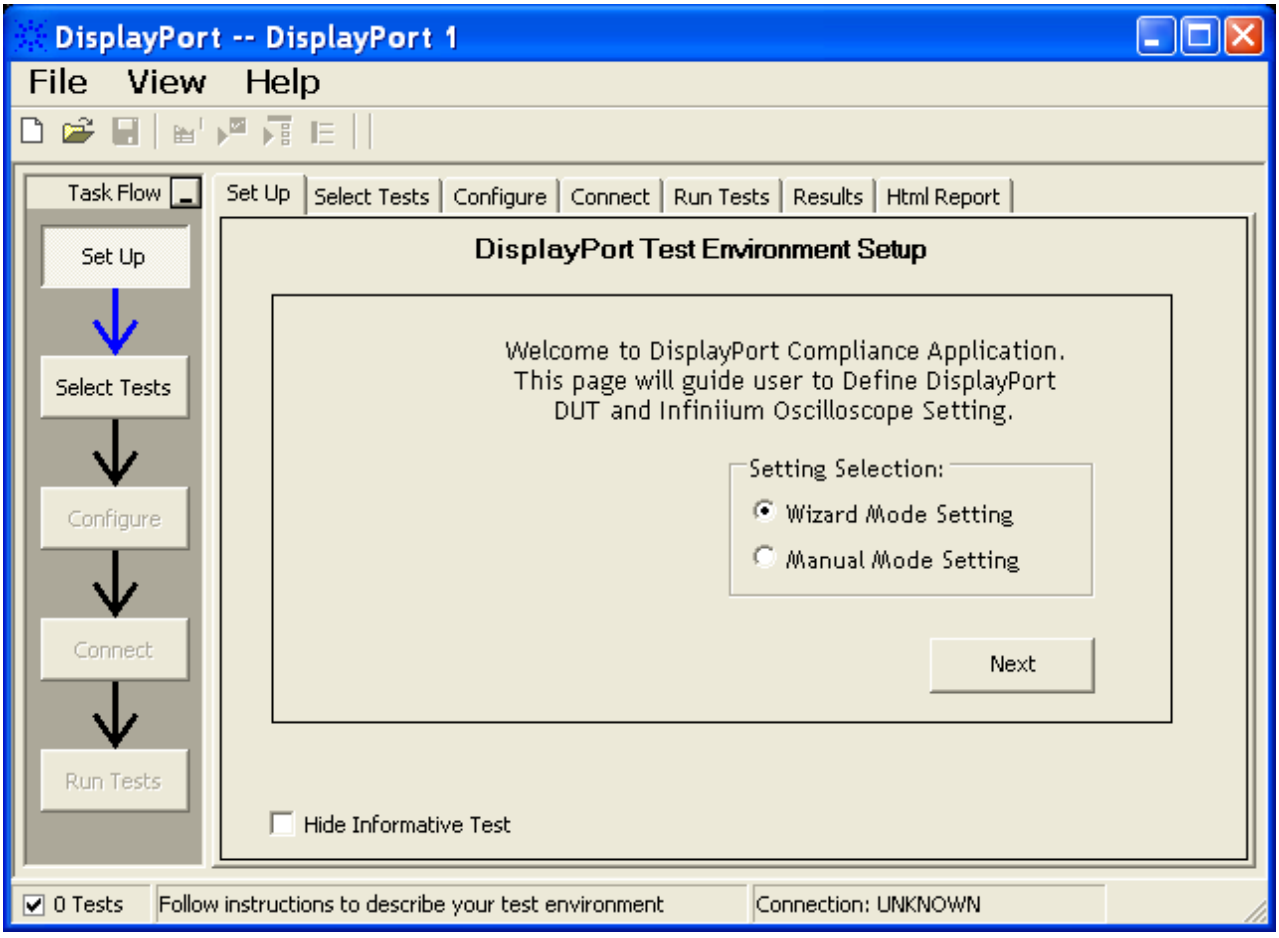

Figure 25 Setup for pre-emphasis level verification Differential Tests (Two Connections with W2641A DisplayPort Test Fixture)

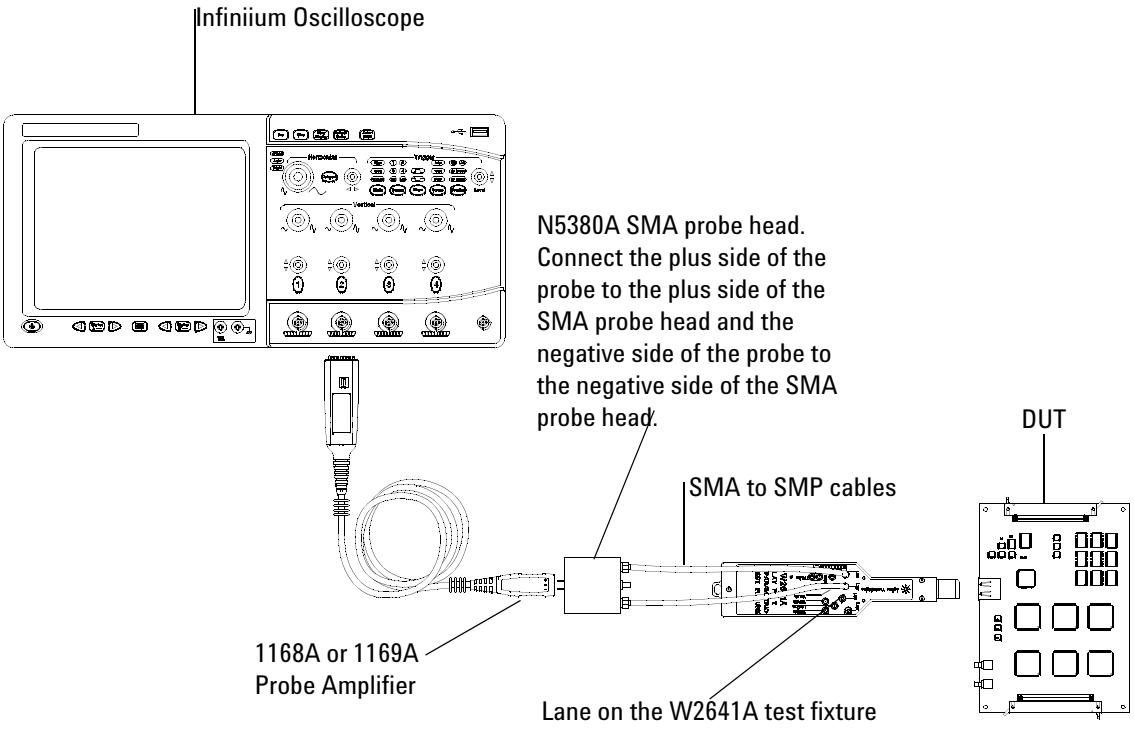

Figure 26 Probing for Differential Tests - Pre-emphasis Level Verification Tests (Two Connections with W2641A DisplayPort Test Fixture)

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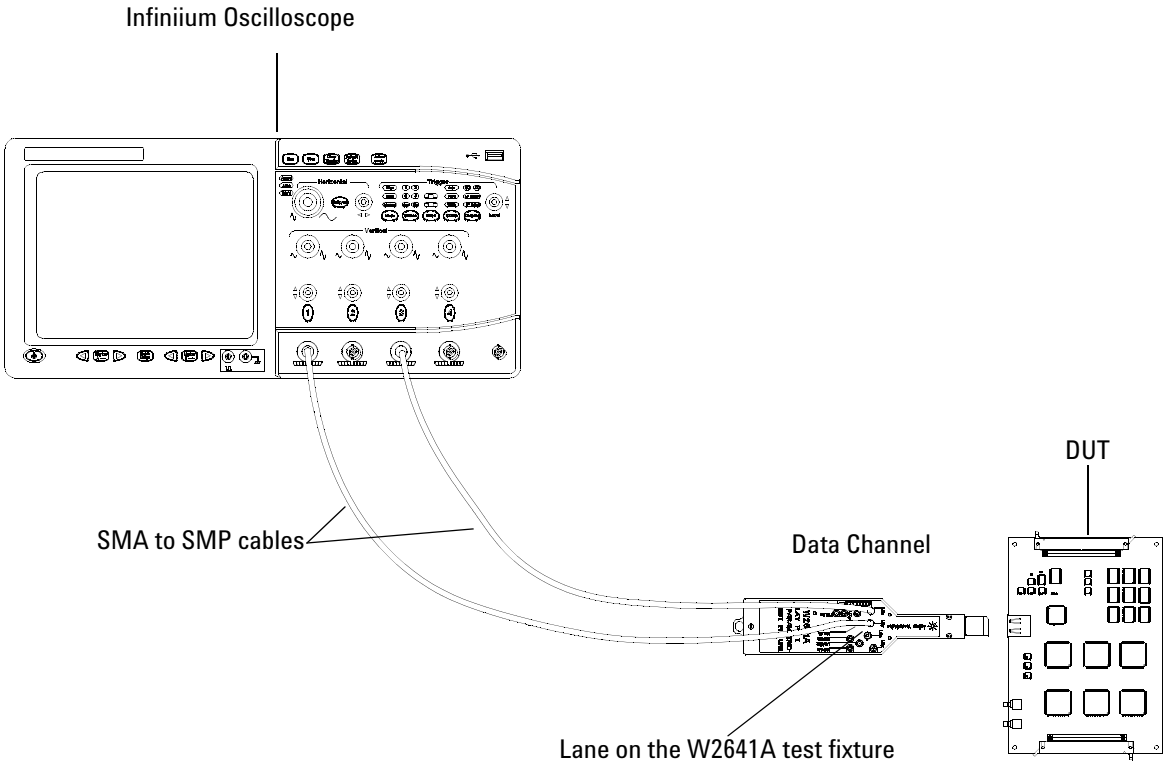

Figure 27 Probing for Single-ended Tests - Pre-emphasis Level Verification Tests (Two Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Pre-emphasis Level Verification Test

This test evaluates the effect of pre-emphasis on the source waveform by measuring the peak differential amplitude and assuring the accuracy of the pre-emphasis setting. (Reference: Table 3.10 VESA DisplayPort Standard)

The source can apply pre-emphasize to the waveform in order to overcome the harmful effects caused by such things as system losses through pc boards, connectors, and cables. The standard stipulates the relative magnitude to overcome specific losses. Because pre-emphasis is negotiated, two units with substantially different degrees of pre-emphasis may be seen as non-interoperable under certain conditions. This test ensures that the system loss or pre-emphasis budget is obeyed.

Tests must be made on all bit rates supported with pre-emphasis for all differential voltage swings supported using a test pattern of PRMS 7. The following equation is used to calculate the pre-emphasis result:

$$\text{Pre-emphasis Result} = 20\log\left(\frac{V_{Swingpe}}{V_{Swingnope}}\right)$$

$$V_{Swingpe} = (V_{Hpe} - V_{Lpe})$$

$$V_{Swingnope} = (V_{Hnope} - V_{Lnope})$$

where:

V_{Hpe} = the high voltage value is measured using the histogram modes at the top for transition eyes.

V_{Lpe} = the low voltage value is measured using the histogram modes at the top for transition eyes.

V_{Hnope} = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

V_{Lnope} = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two

channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.

4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.

5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.

6 In the DisplayPort Compliance Test Application, click the Set Up tab.

7 Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

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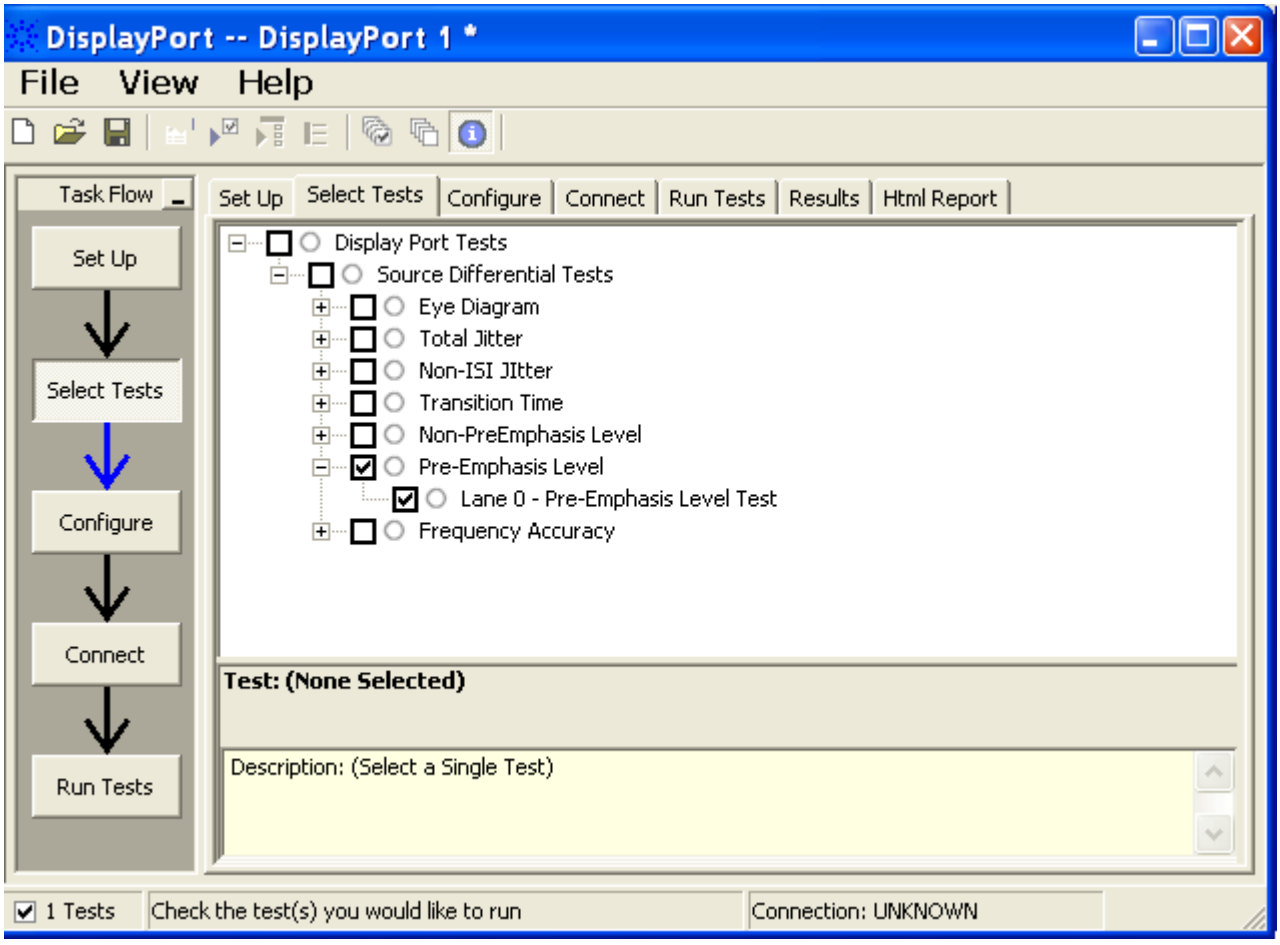

Figure 28 Selecting Pre-emphasis Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 9), make oscilloscope connections, run the tests, and view the test results.

Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 9 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 9 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 9 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

The pre-emphasis calculation must fall within the following ranges for each pre-emphasis level:

3.5 dB setting: 2.8 dB ≤ Result ≤ 4.2 dB

6.0 dB setting: 4.8 dB ≤ Result ≤ 7.2 dB

9.5 dB setting: 7.6 dB ≤ Result ≤ 11.4 dB

Test References

See Test 3-3: Pre-emphasis Level Verification Testing, in the *DisplayPort-Compliance Test Specification Version 1.*

9 Source Frequency Accuracy Tests

This section provides the guidelines for source frequency accuracy differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

NOTE Agilent Option 001 (1M/ch memory upgrade) is recommended; this will greatly reduce frequency accuracy test time.

Probing for Frequency Accuracy Tests

When performing the frequency accuracy test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 29 below: two Connection by using W2641A Test Fixture, then your physical connection for the frequency accuracy test should be similar to Figure 30.

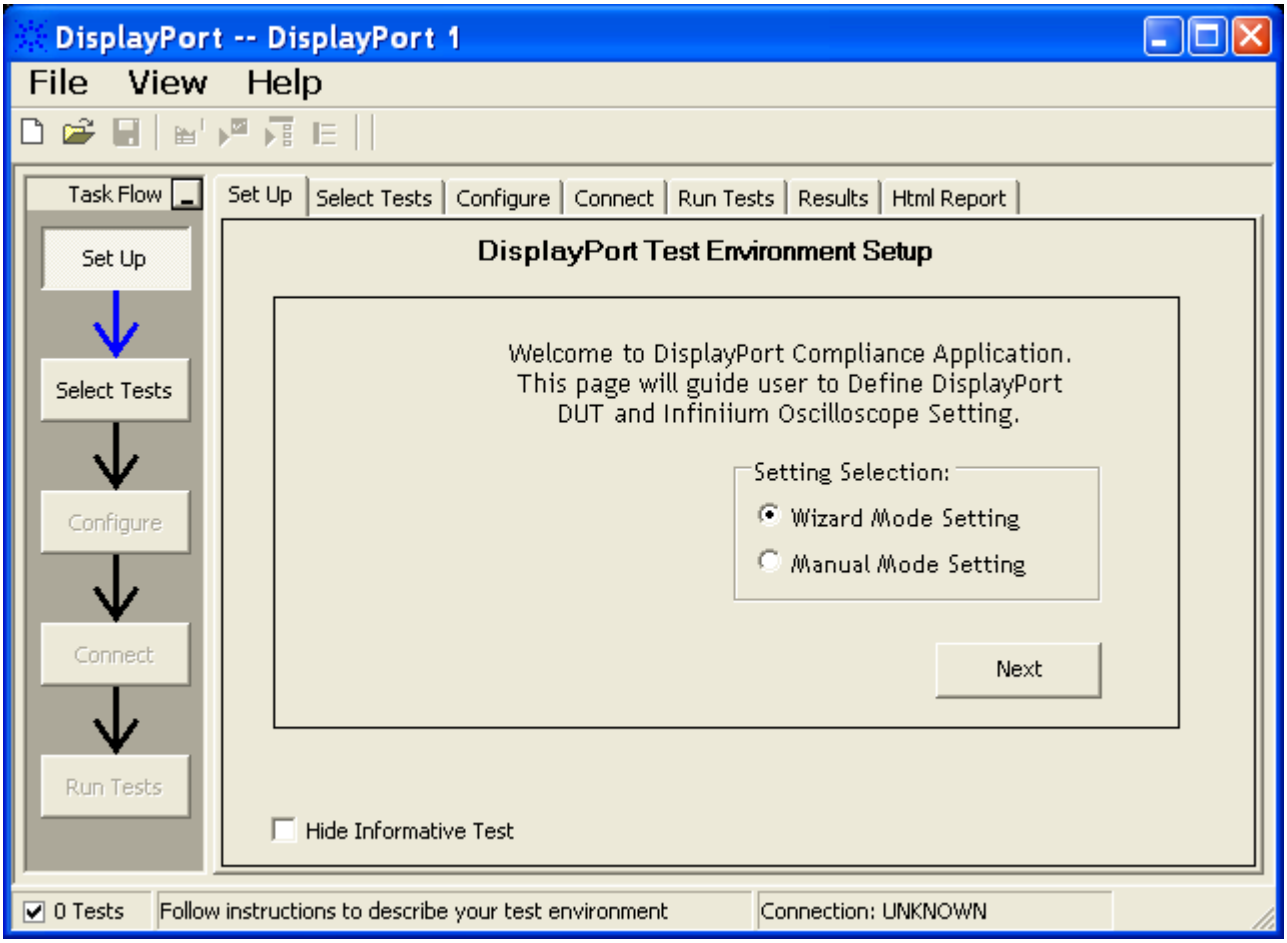

Figure 29 Setup for Frequency Accuracy Differential Tests (Two Connections with W2641A DisplayPort Test Fixture)

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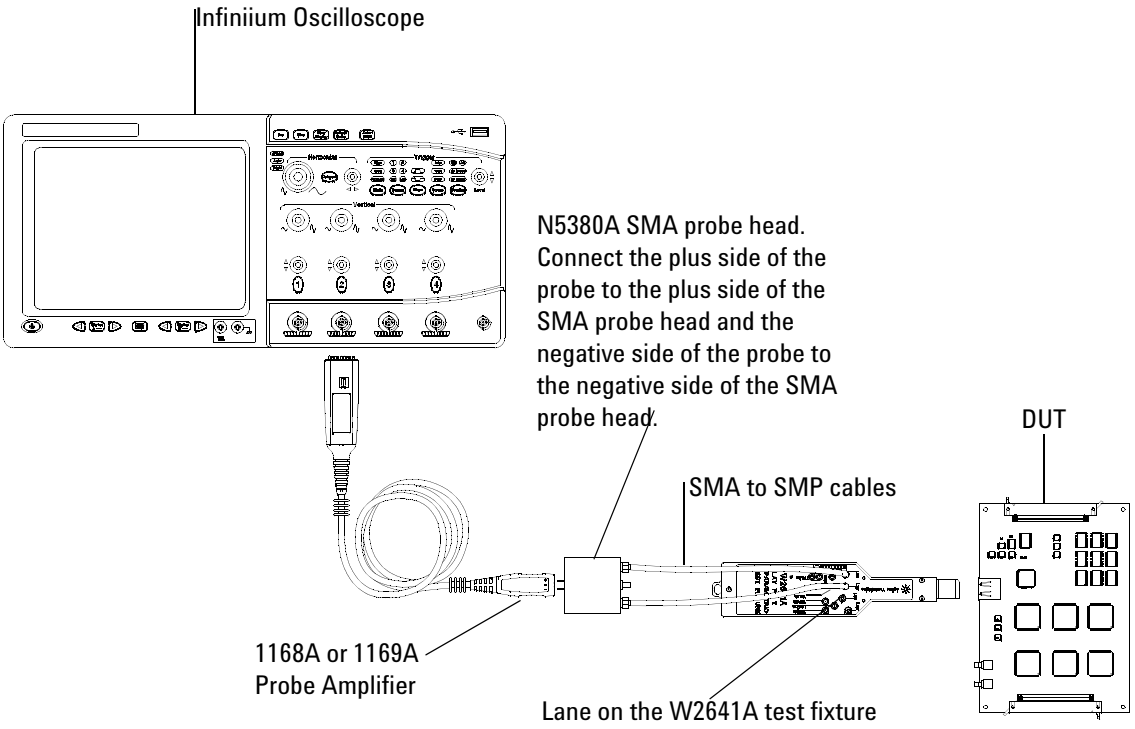

Figure 30 Probing for Single-ended Tests - Frequency Accuracy Tests (Two Connections with W2641A DisplayPort Test Fixture)

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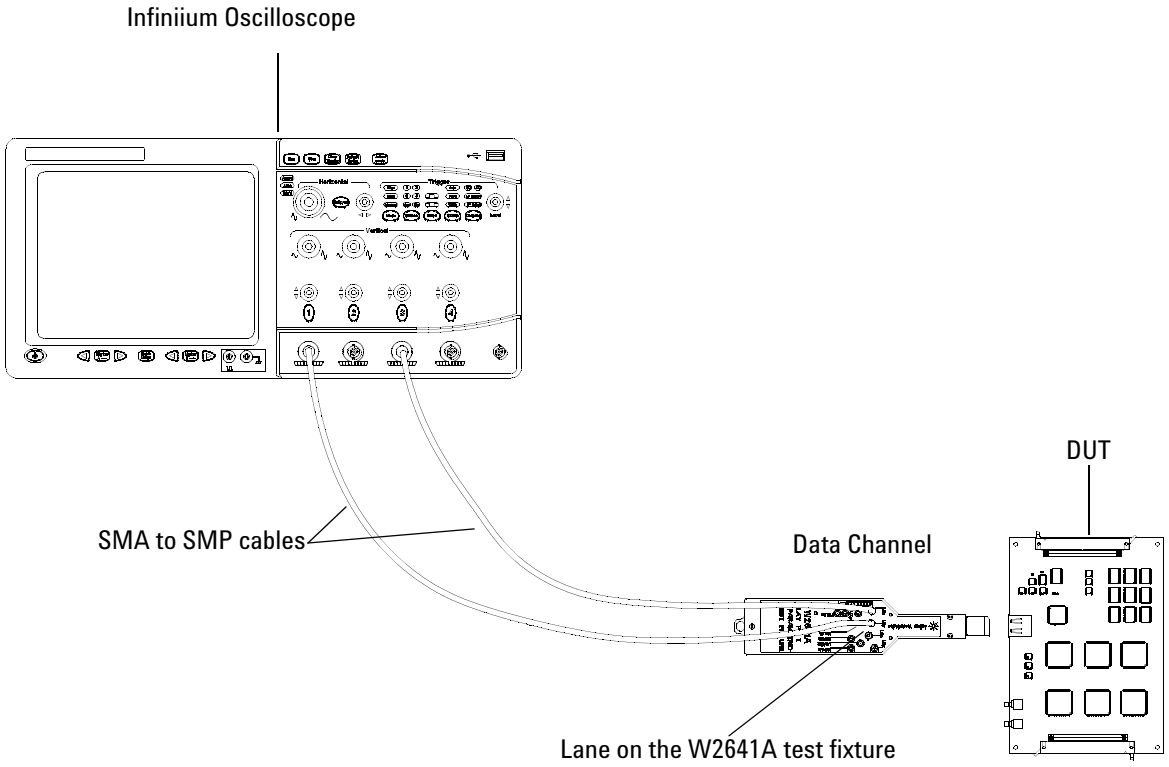

Figure 31 Probing for Differential Tests - Frequency Accuracy Tests (Two Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Frequency Accuracy Test

The frequency accuracy measurement of the distributed clock network verifies that the nominal operating clock frequency is within the acceptable tolerance range. In order for sink devices to properly recover the data, the source clock must operate within the acceptable tolerance range.

The test must be made at all bit rates supported by the device under test without pre-emphasis and a voltage swing of 1.2 volts. A test pattern of D10.2 should be used.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the Frequency Accuracy group, and check the lanes that you want to perform.

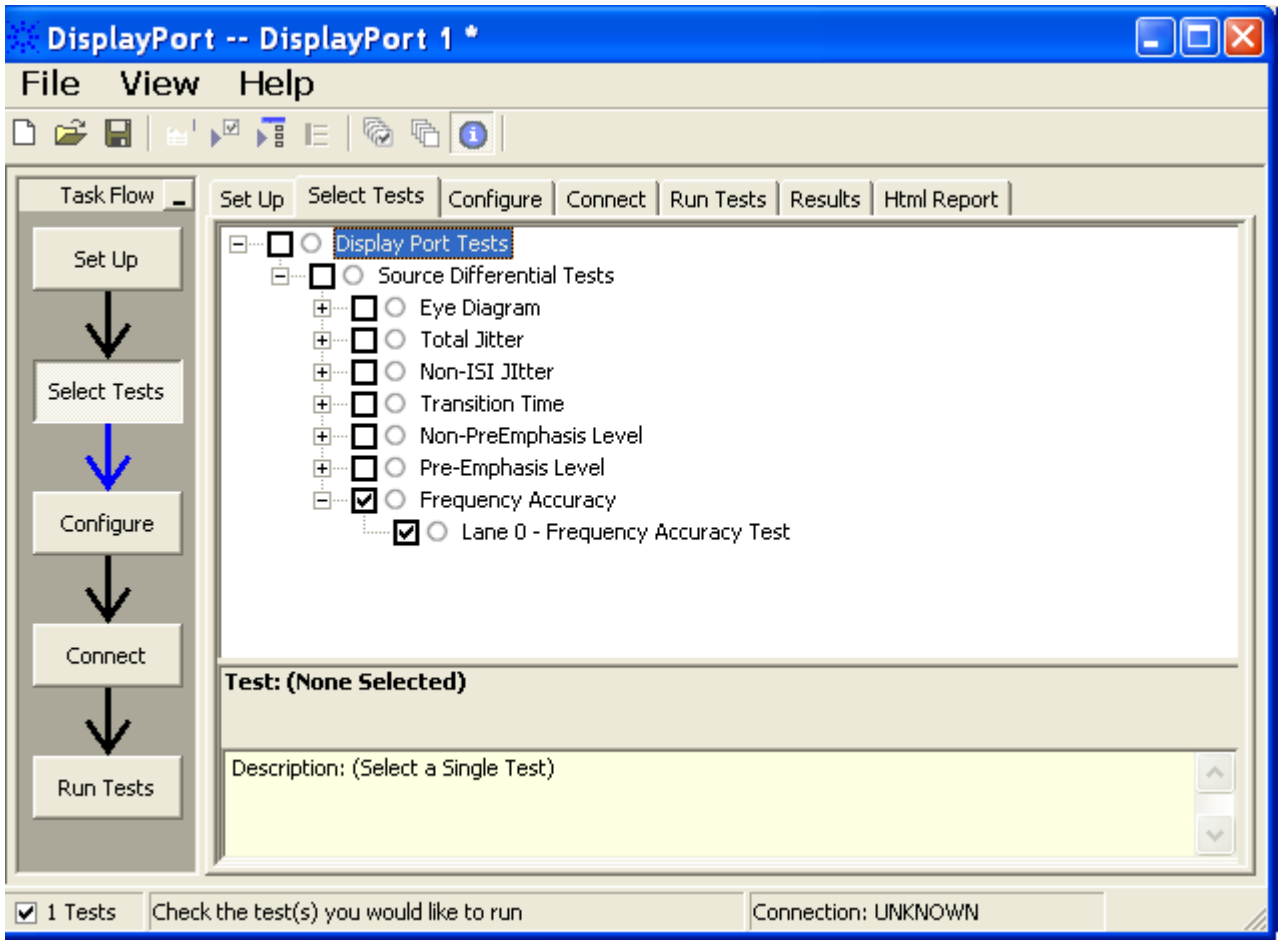

Figure 32 Selecting Transition Time Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 10), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 10 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL; ζ = the dampling factor of the PLL; F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 10 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 10 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

Frequency Accuracy = Nominal Frequency ±300 ppm.

Test References

See Test 3.9: Frequency Accuracy, in the *DisplayPort- Compliance Test Specification Version 1*.

10 Source Inter-Pair Skew Tests

This section provides the guidelines for source inter-pair skew single-ended tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Inter-Pair Skew Single-ended Tests

When performing the inter-pair skew test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 33 below: two Connection by using W2641A Test Fixture, then your physical connection for the inter-pair skew test should be similar to Figure 34

.

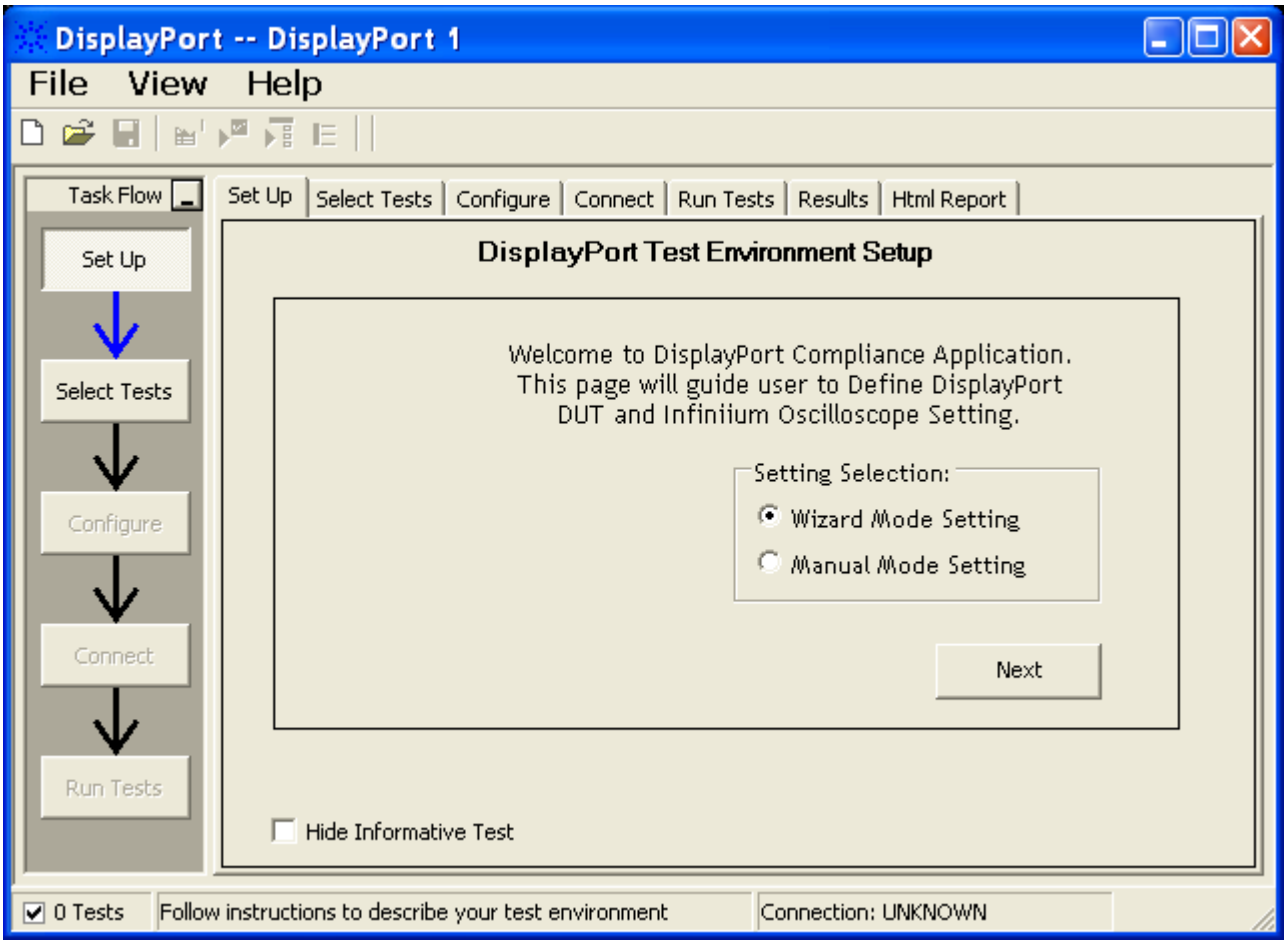

Figure 33 Setup for Inter-Pair Skew Differential Tests (Two Connections with W2641A DisplayPort Test Fixture)

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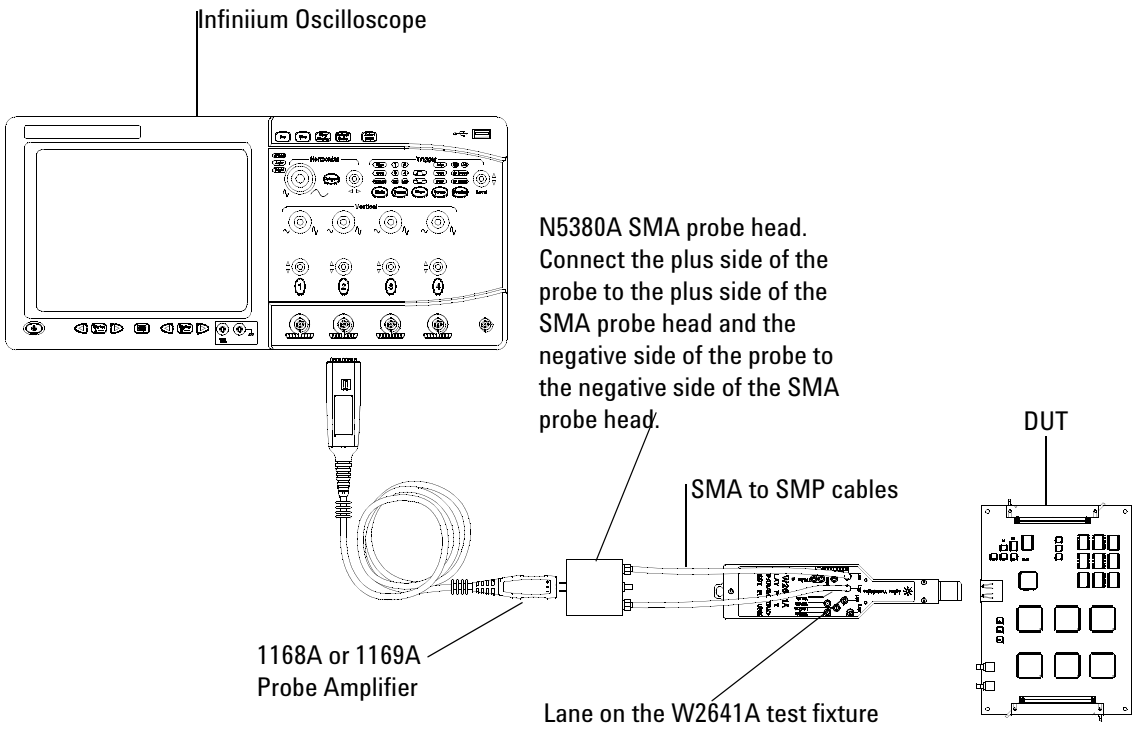

Figure 34 Probing for Differential Tests - Inter-Pair Skew Tests (Two Connections with W2641A DisplayPort Test Fixture)

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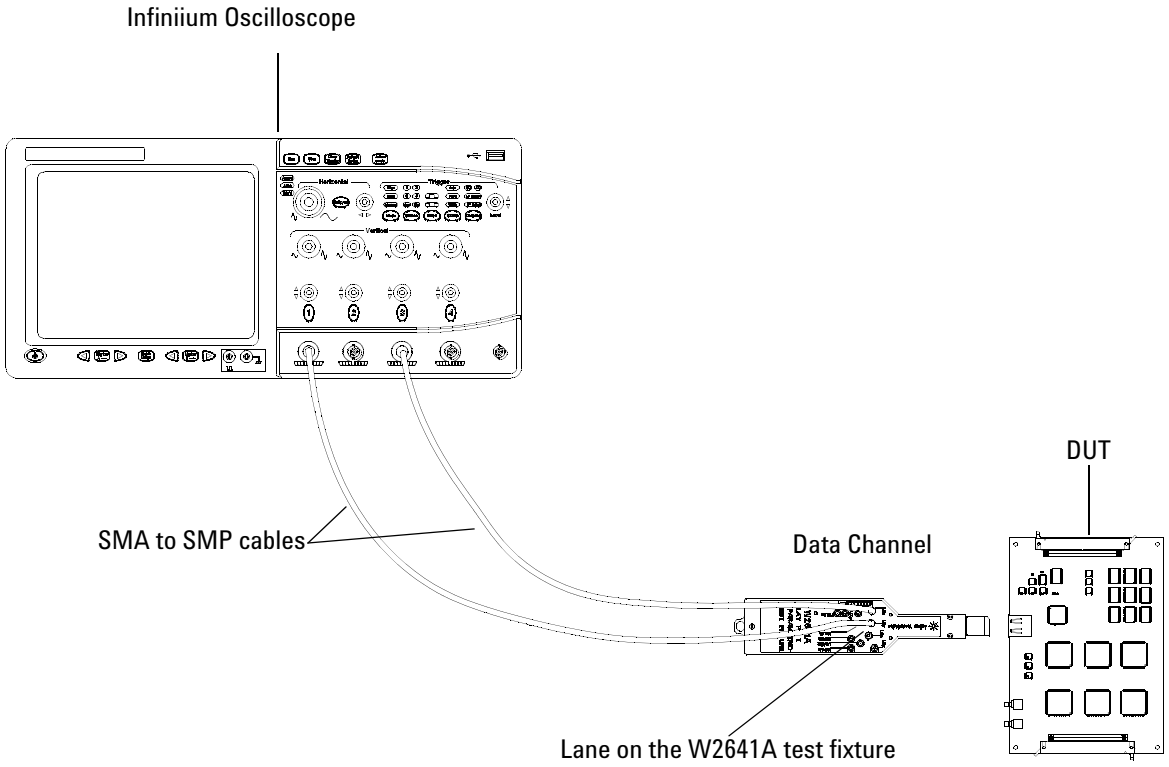

Figure 35 Probing for Single-ended Tests - Inter-Pair Skew Tests (Two Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Inter-Pair Skew Test

The inter-pair skew test evaluates the skew, or time delay, between respective differential data lanes in the DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard)

The DisplayPort interface has the ability to skew, or deskew lanes by 20 UI (Unit Intervals) which is as much as 12ns (1.62Gb/s) and is intended to eliminate simultaneous degradation of concurrent bytes of transmitted data. The specification at 150 ps at the package pins(TP1), likely to be degraded another 50 ps through the connector, is less than 0.5 UI at the highest bit rate. Therefore, it is unlikely to be a significant reason for non-interoperability.

Channel-to-channel de-skew must be performed on the two oscilloscope channels used for this measurement (see “Differential Probe Head Skew Calibration" on page 139 and “SMA Probe Head Skew Calibration" on page 145).

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the Inter-pair Skew Test group, and check the rise time and fall time tests that you want to perform.

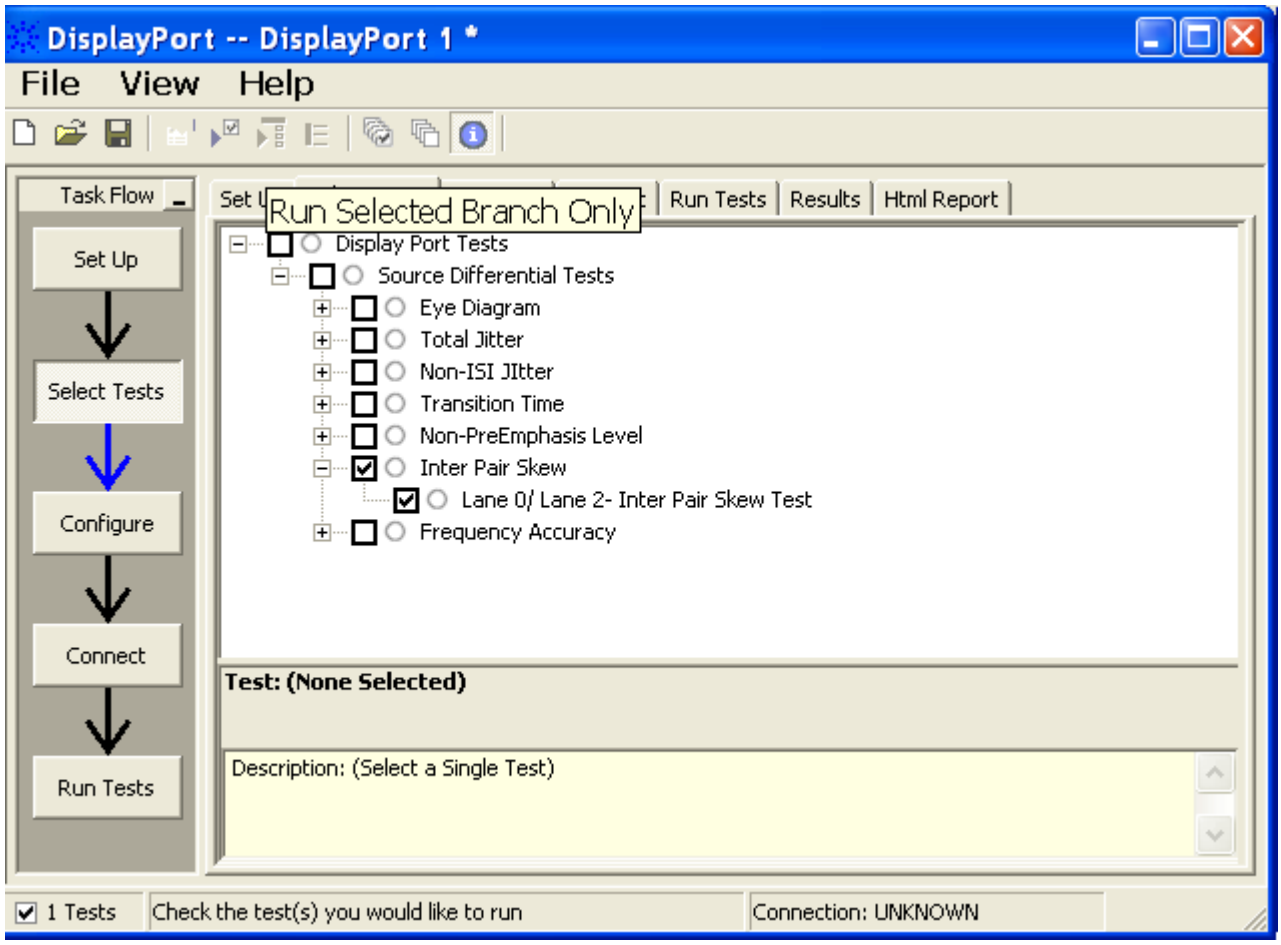

Figure 36 Selecting Transition Time Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 11), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 11 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL; ζ = the dampling factor of the PLL; F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 11 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 11 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

Inter-Pair Skew ≤ 2 UI

Test References

See Test 3.4: Inter-Pair Skew Measurement, in the *DisplayPort-Compliance Test Specification Version 1.*

11 Source Rise And Fall Time Mismatch Tests

This section provides the guidelines for source transition time tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Single-ended Tests

When performing the transition time test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 37 below: two Connection by using W2641A Test Fixture, then your physical connection for the transition time test should be similar to Figure 38.

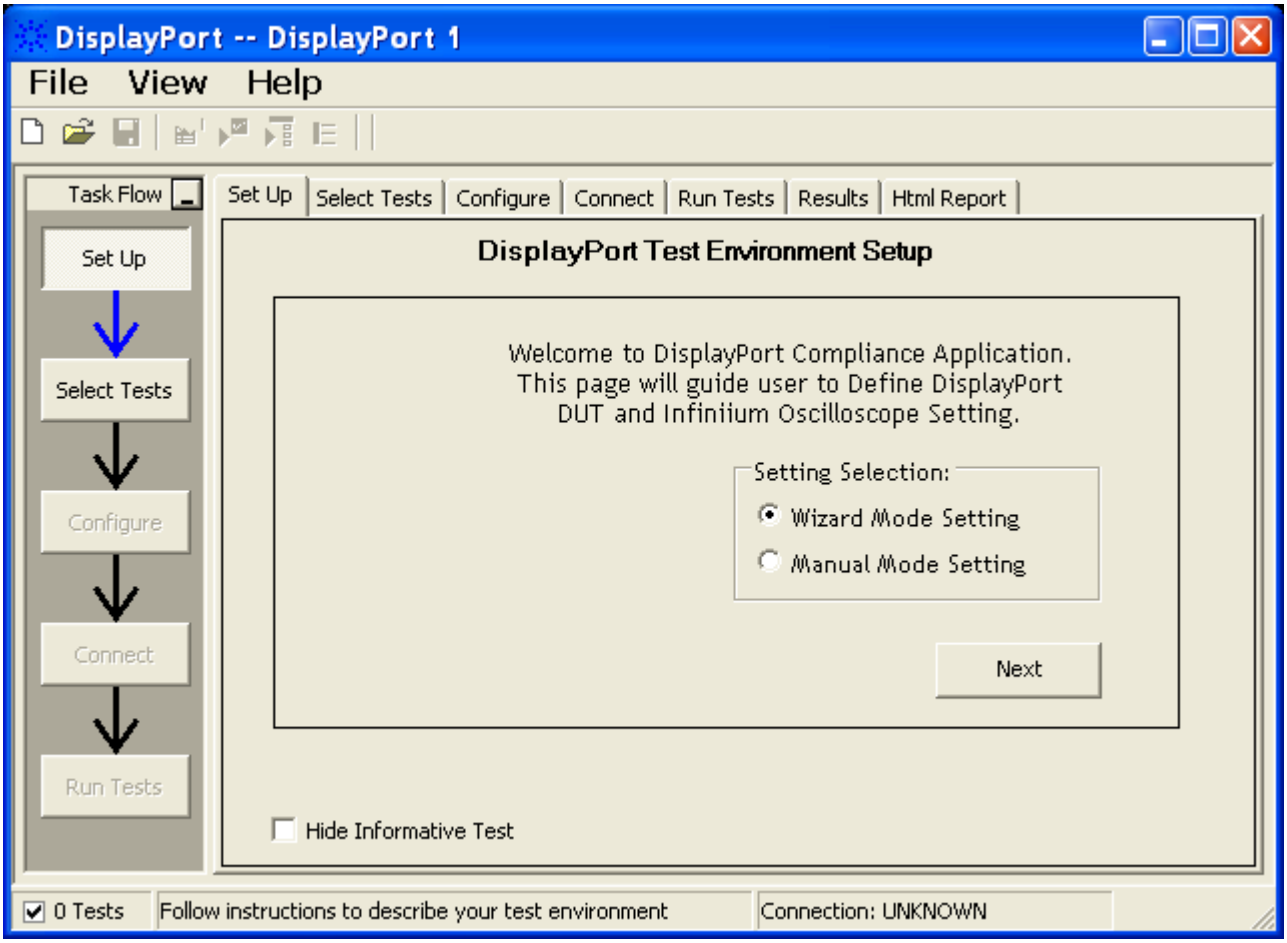

Figure 37 Setup for Rise And Fall Time Mismatch Tests (Two Connections with W2641A DisplayPort Test Fixture)

Figure 38 and Figure 39 below show the single-ended and differential connections for Transition Time Tests.

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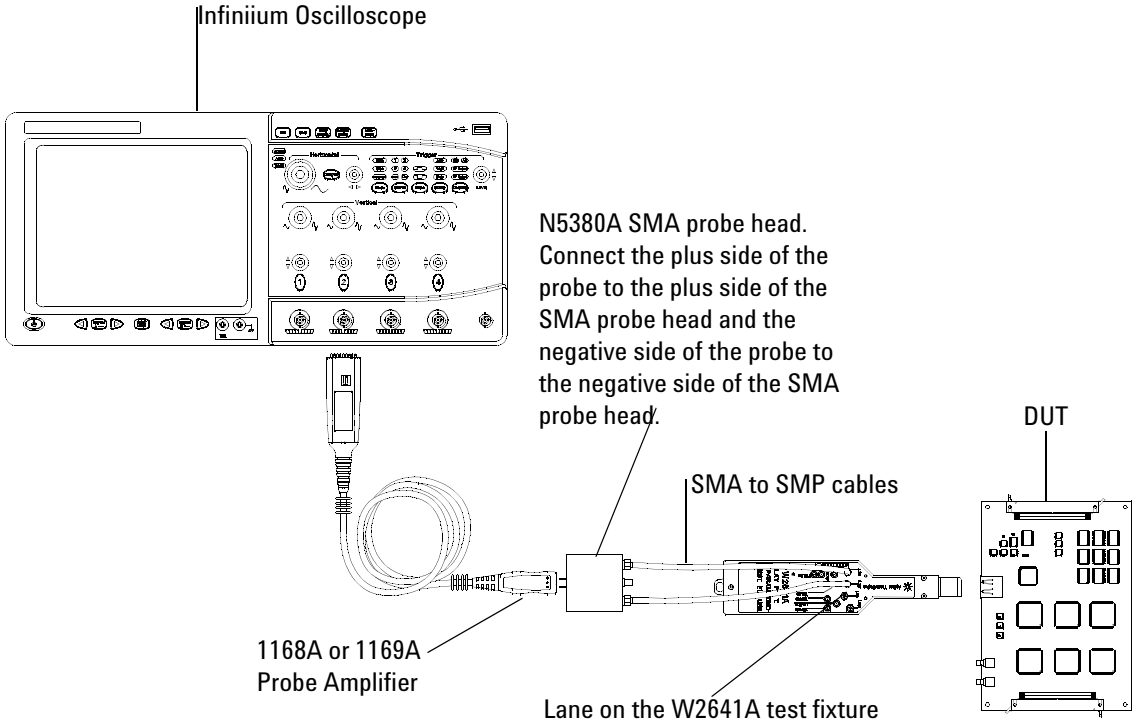

Figure 38 Probing for Differential Tests - Transition Time Tests (Two Connections with W2641A DisplayPort Test Fixture)

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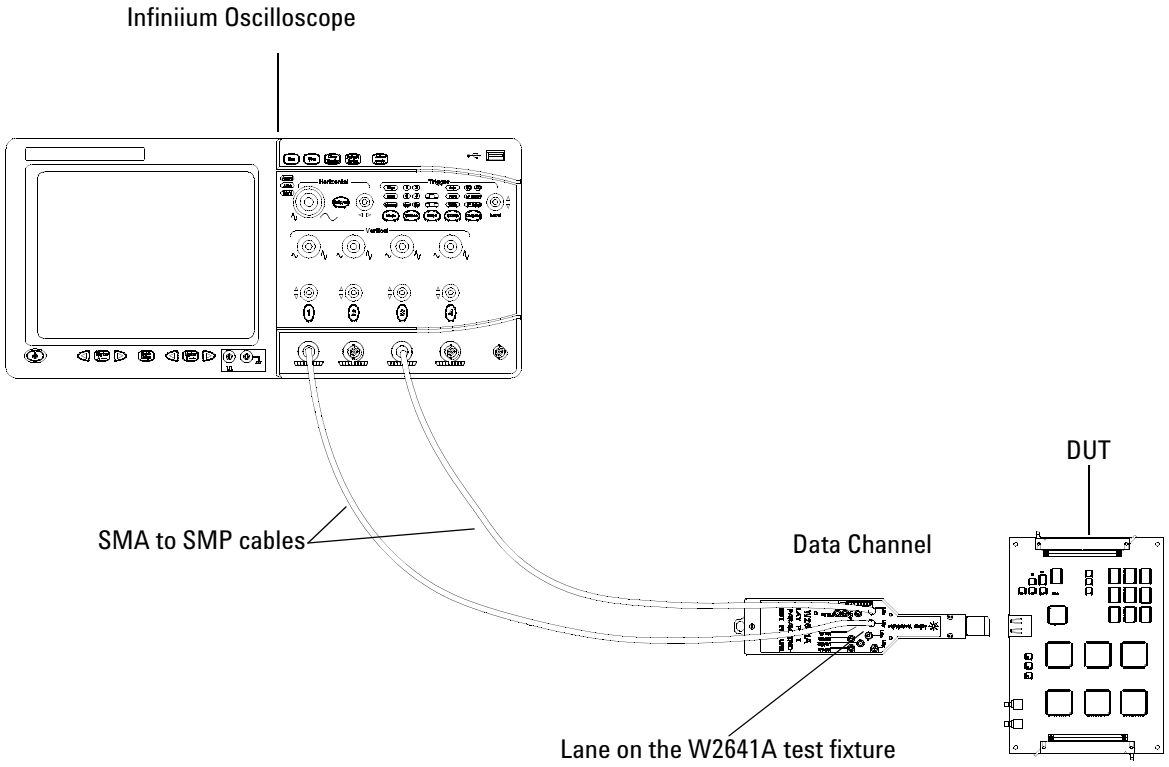

Figure 39 Probing for Single-ended Tests - Rise and Fall Time Mismatch Tests (Four Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Rise And Fall Time Mismatch Tests

The rise and fall time mismatch tests evaluate the difference in rise and fall times of the two single-ended waveform in a given differential data lane of a DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard specification.)

The mismatch in time of the rising and falling time of the single-ended signals composing a differential lane will create common mode noise and will radiate.

The rise and fall times are measured between the 80% and 20% levels of the waveform.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the Rise-Fall Mismatch group, and check the Rising Mismatch and Falling Mismatch tests that you want to perform.

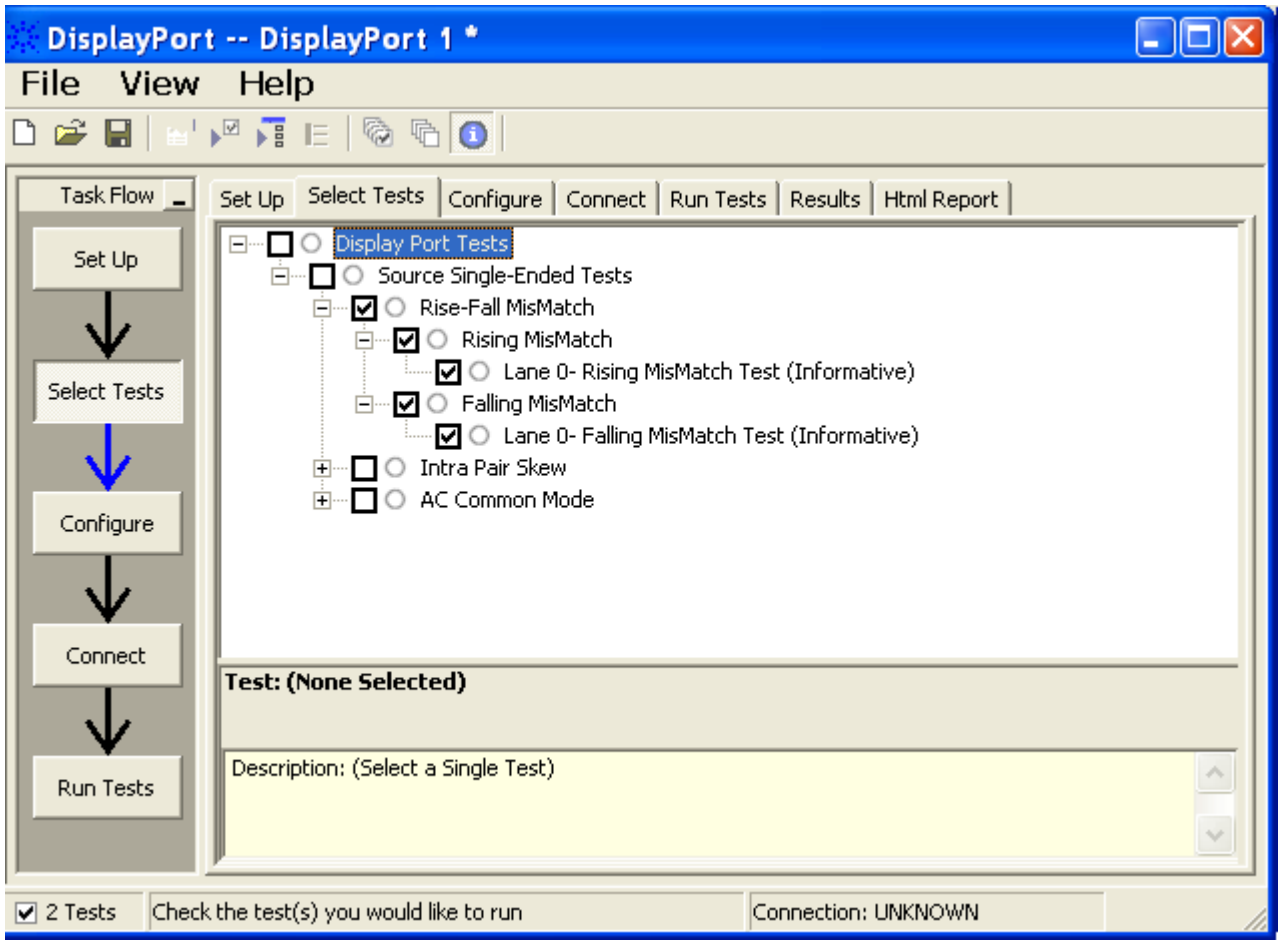

Figure 40 Selecting Rise And Fall Time Mismatch Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 12), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 12 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL; ζ = the dampling factor of the PLL; F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 12 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 12 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

Falling Mismatch ≤ 15% of the single-ended rise time
Rising Mismatch ≥ 15% of the single-ended fall time

Test References

See section 3.7, in the *DisplayPort-Compliance Test Specification Version 1*.

11 Source Rise And Fall Time Mismatch Tests

12
Source Intra-Pair Skew Tests

This section provides the guidelines for source intra-pair skew tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

Probing for Single-Ended Tests

When performing the intra-pair skew test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 41 below: two Connection by using W2641A Test Fixture, then your physical connection for the data eye test should be similar to Figure 42.

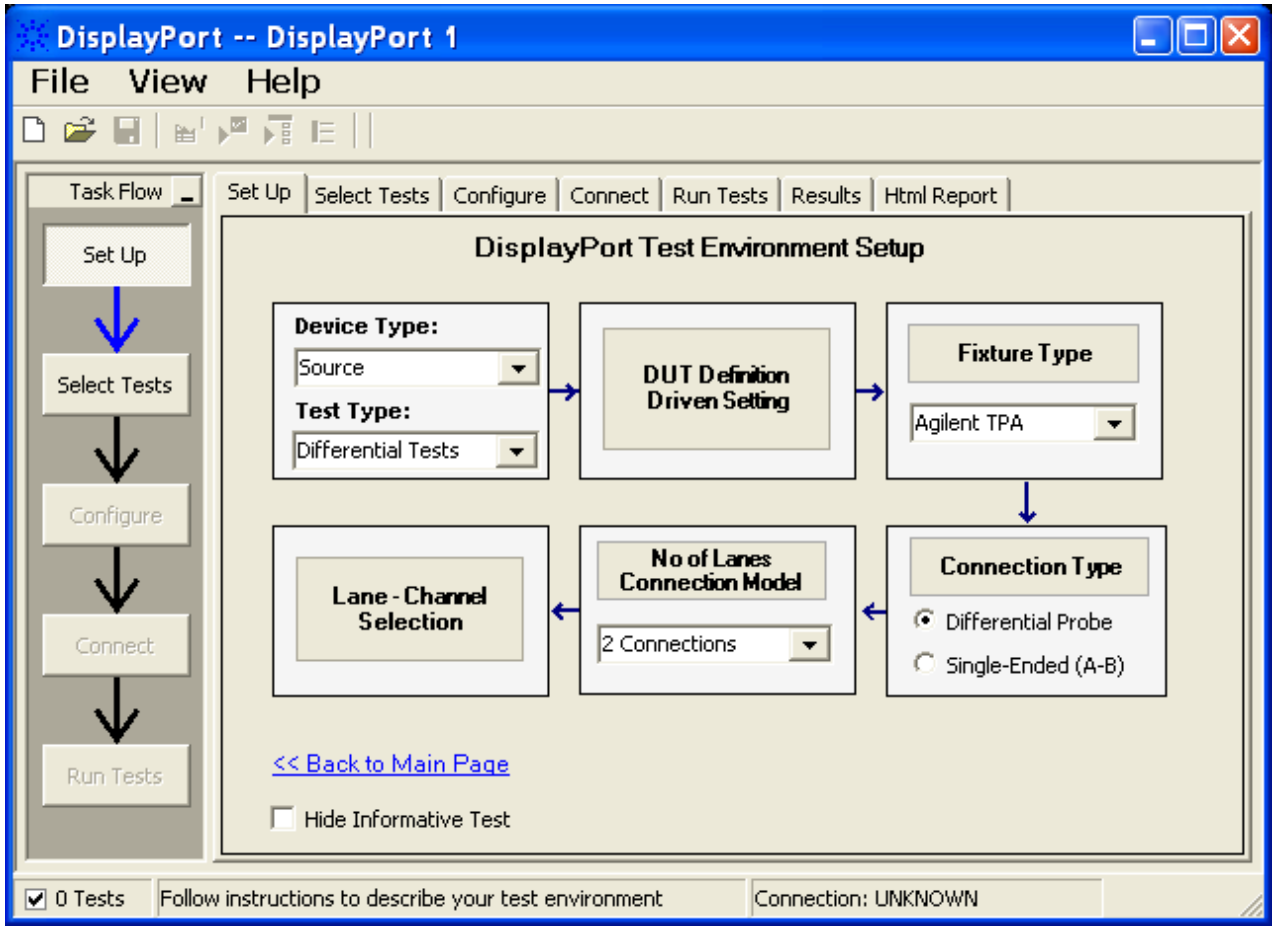

Figure 41 Setup for Intra-pair Skew Differential Tests (Two Connections with W2641A DisplayPort Test Fixture)

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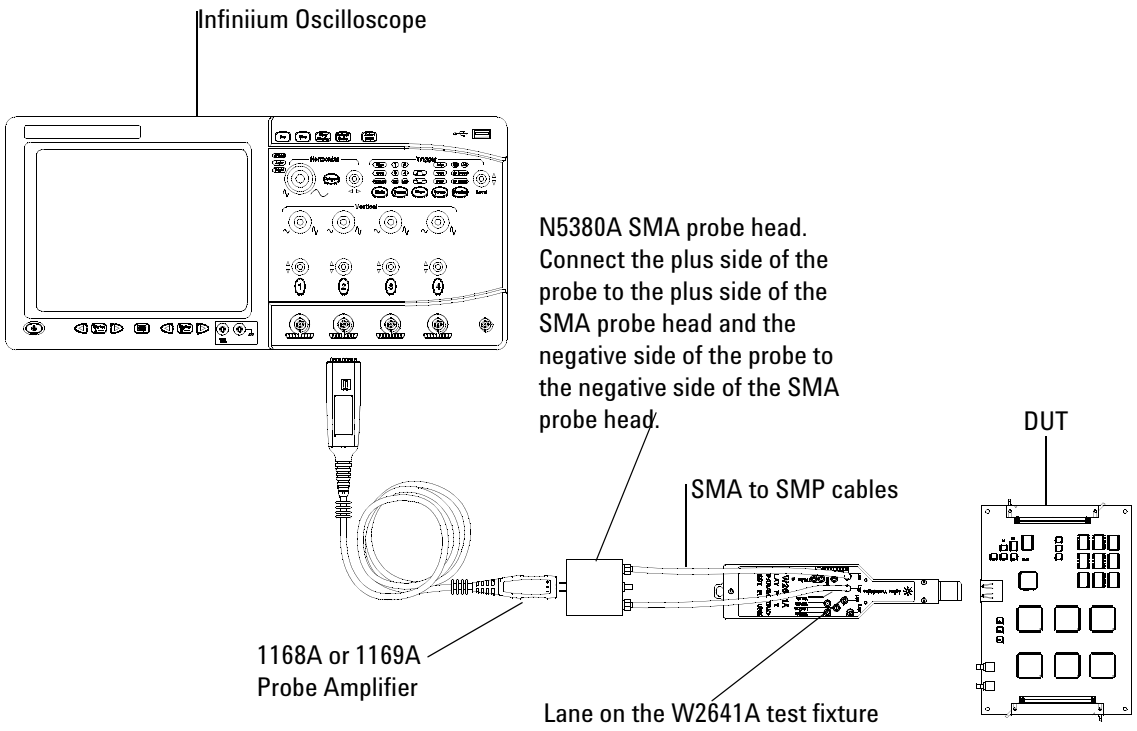

Figure 42 Probing for Differential - Intra-pair Skew Tests (Two Connections with W2641A DisplayPort Test Fixture)

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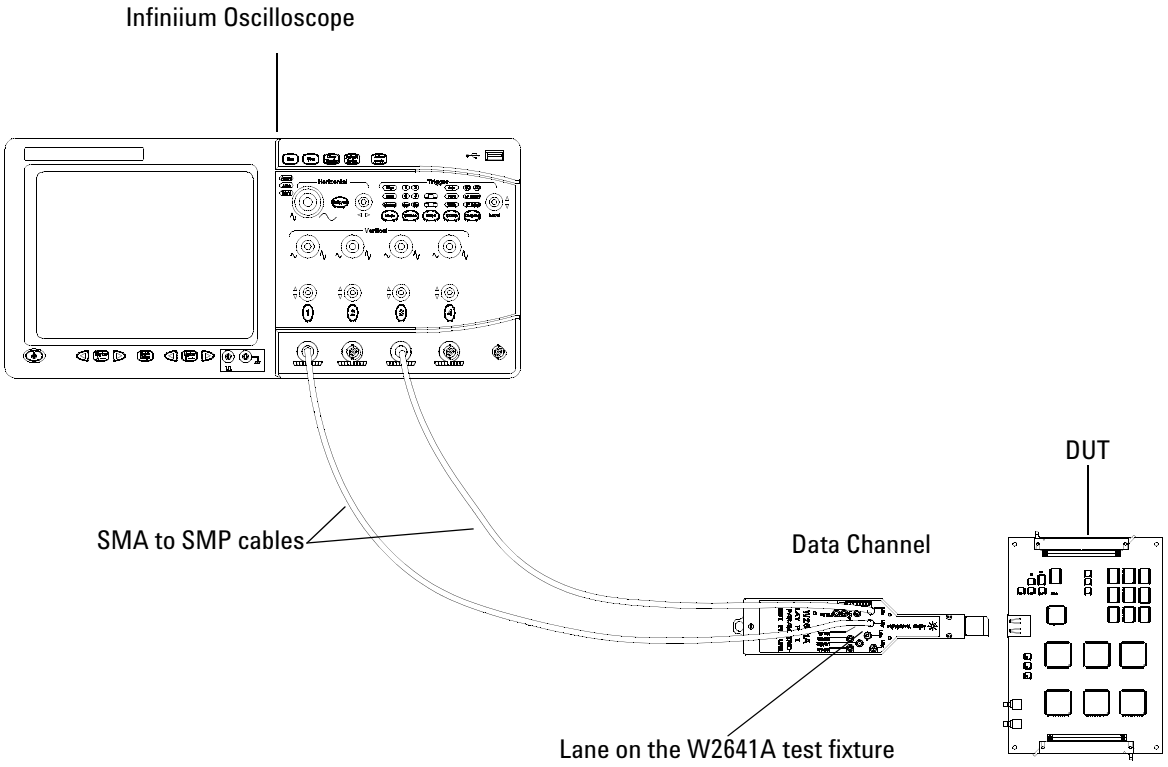

Figure 43 Probing for Single-ended Tests - Inter-Pair Skew Tests (Two Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Intra-Pair Skew Test

The intra-pair skew test evaluates the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard)

Intra-pair skew has deleterious effects on signal rise time and manner of crossing through the transition point. The DisplayPort specification at package pins (TP1) is 20 ps. It can clearly double or triple to and through the connector. These are secondary contributors to source jitter performance.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the Intra-Pair Skew group, and check the lane you want to test.

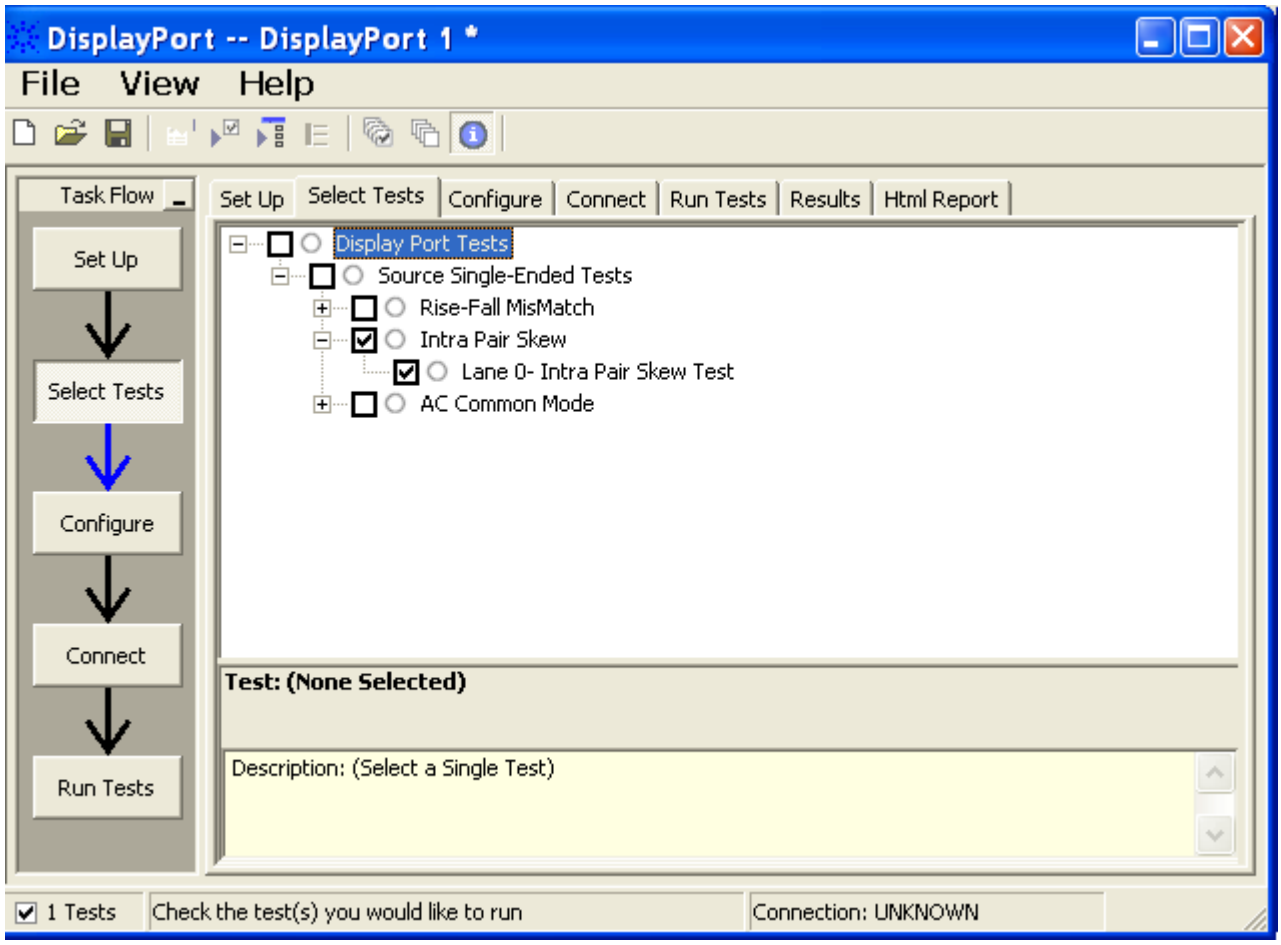

Figure 44 Selecting Intra-pair Skew Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 13), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 13 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL; ζ = the dampling factor of the PLL; F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.

Table 13 Test Configuration Options

Configuration Option	Description
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	

Table 13 Test Configuration Options

Configuration Option	Description
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

Intra-pair Skew ≤ 30 ps

Test References

See Test 3.5: in the *DisplayPort-Compliance Test Specification Version 1.*

13
Source AC Common Mode Noise Tests

This section provides the guidelines for source AC common mode noise differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.

NOTE Agilent Option 001 (1M/ch memory upgrade) is recommended; this will greatly reduce AC common mode noise test time.

Probing for AC Common Mode Noise Tests

When performing the AC common mode noise test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection. There are two modes that you can use to configure the Set Up tab: Wizard Mode and Manual Mode. The Wizard Mode leads you step by step through each of the different setup choices with a description of what the choices do. The Manual Mode allows you to choose only those set up choices that you want to make without going through every possible choice of settings.

For example, if your test environment setup is similar to Figure 45 below: two Connection by using W2641A Test Fixture, then your physical connection for the data eye test should be similar to Figure 46.

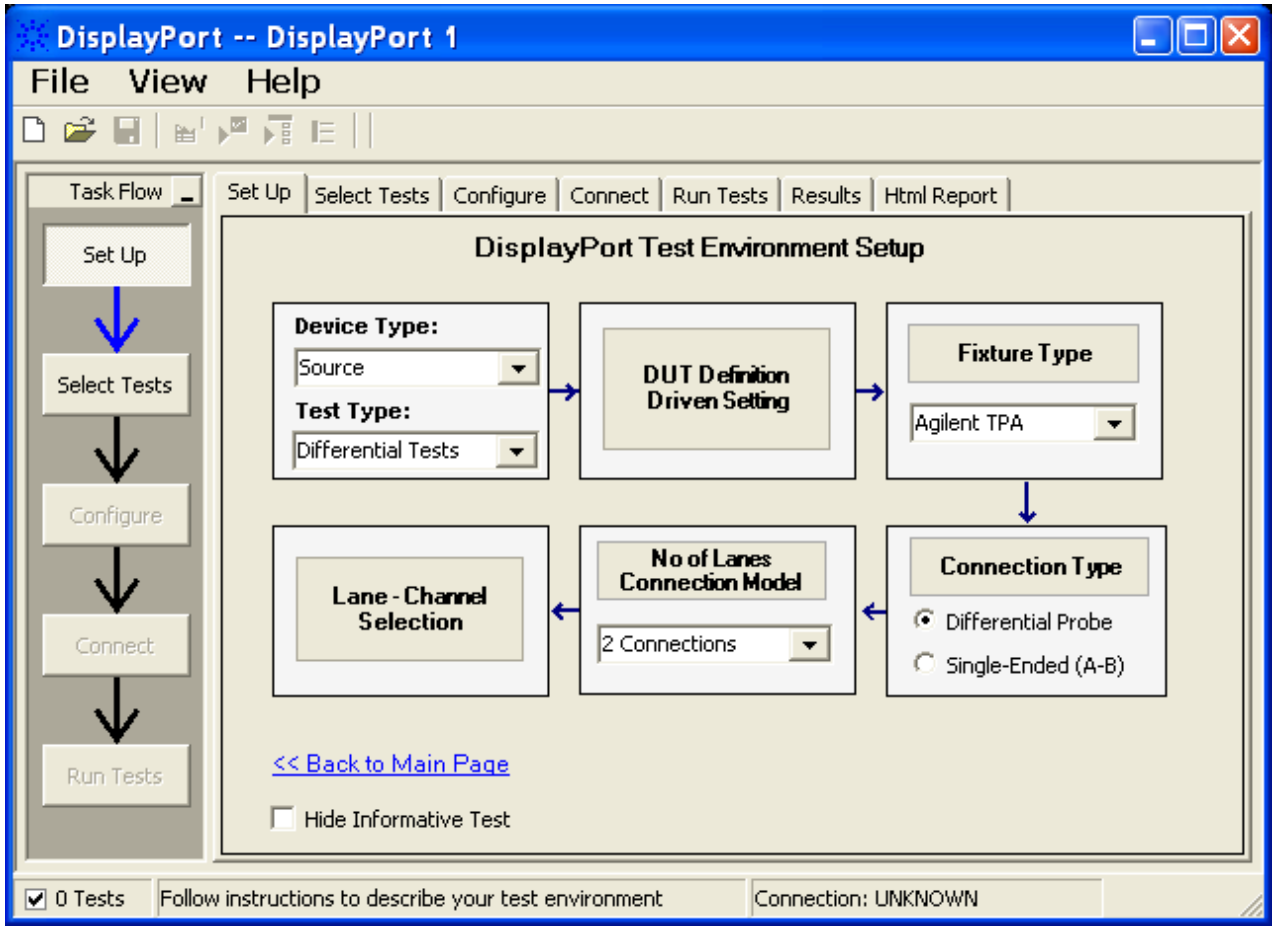

Figure 45 Setup for Data Eye Pattern Differential Tests (Two Connections with W2641A DisplayPort Test Fixture)

Figure 46 shows a physical connection for making single-ended connections.

2641A

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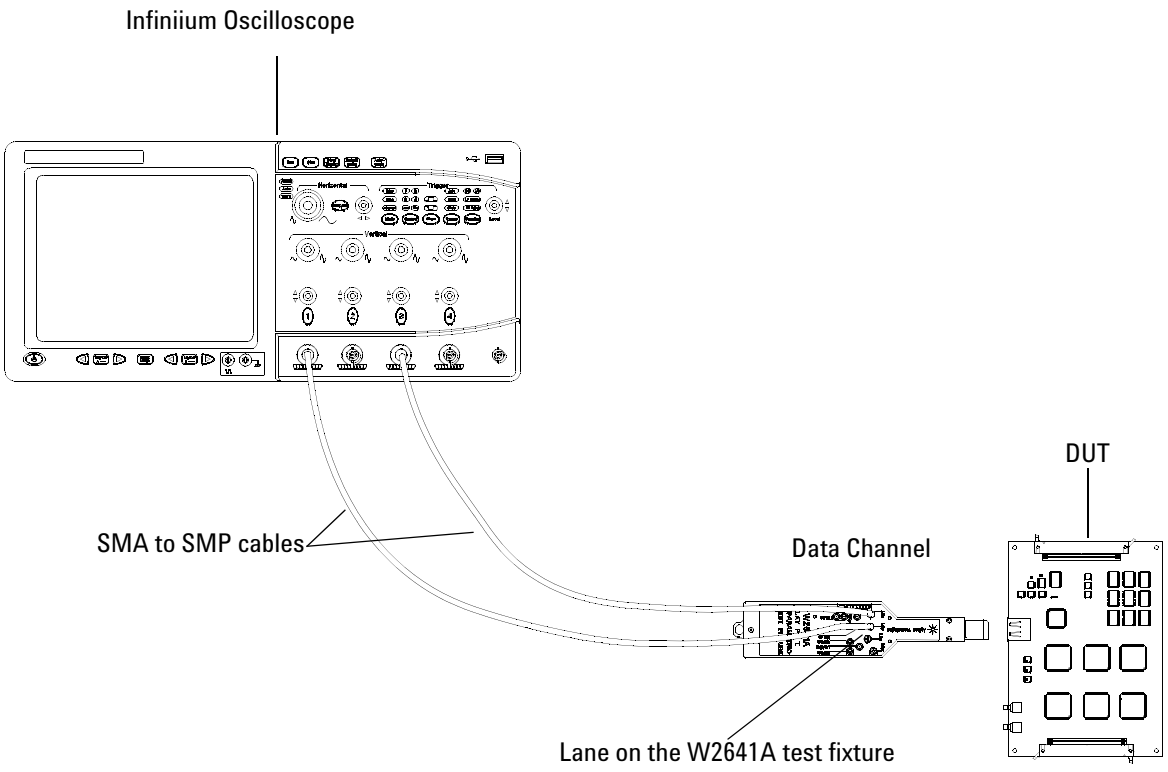

Figure 46 Probing for Single-ended Tests - AC Common Mode Noise Tests (Two Connections with W2641A DisplayPort Test Fixture)

You can use any of the oscilloscope channel and connect them to any of the lane test points. You select the channels used for test a lane in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

AC Common Mode Noise Test

The AC common mode noise measurement of the distributed clock network verifies that the nominal operating clock frequency is within the Acceptable tolerance range. In order for sink devices to properly recover the data, the source clock must operate within the Acceptable tolerance range.

The test must be made at all bit rates supported by the device under test without pre-emphasis and a voltage swing of 1.2 volts. A test pattern of D10.2 should be used.

Test Procedure

1. Start the automated testing application as described in “Starting the DisplayPort Electrical Performance Compliance Test Application" on page 18.
2. Connect the W2641A test fixture to the device under test (DUT).
3. If you are using one connection, connect the probe to any channel. If you are using two connections, connect the two probes to any two channels of the oscilloscope. If you are using four connections, connect the four probes to any four channels of the oscilloscope.
4. Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
5. Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
6. In the DisplayPort Compliance Test Application, click the Set Up tab.
7. Set the DUT Definition Driven Setting, the Test Type, the Fixture Type, Lane-Channel Selection, Connection Settings, and the Connection Type according to the type of testing being done.

Navigate to the AC Common Mode group, and check the rise time and fall time tests that you want to perform.

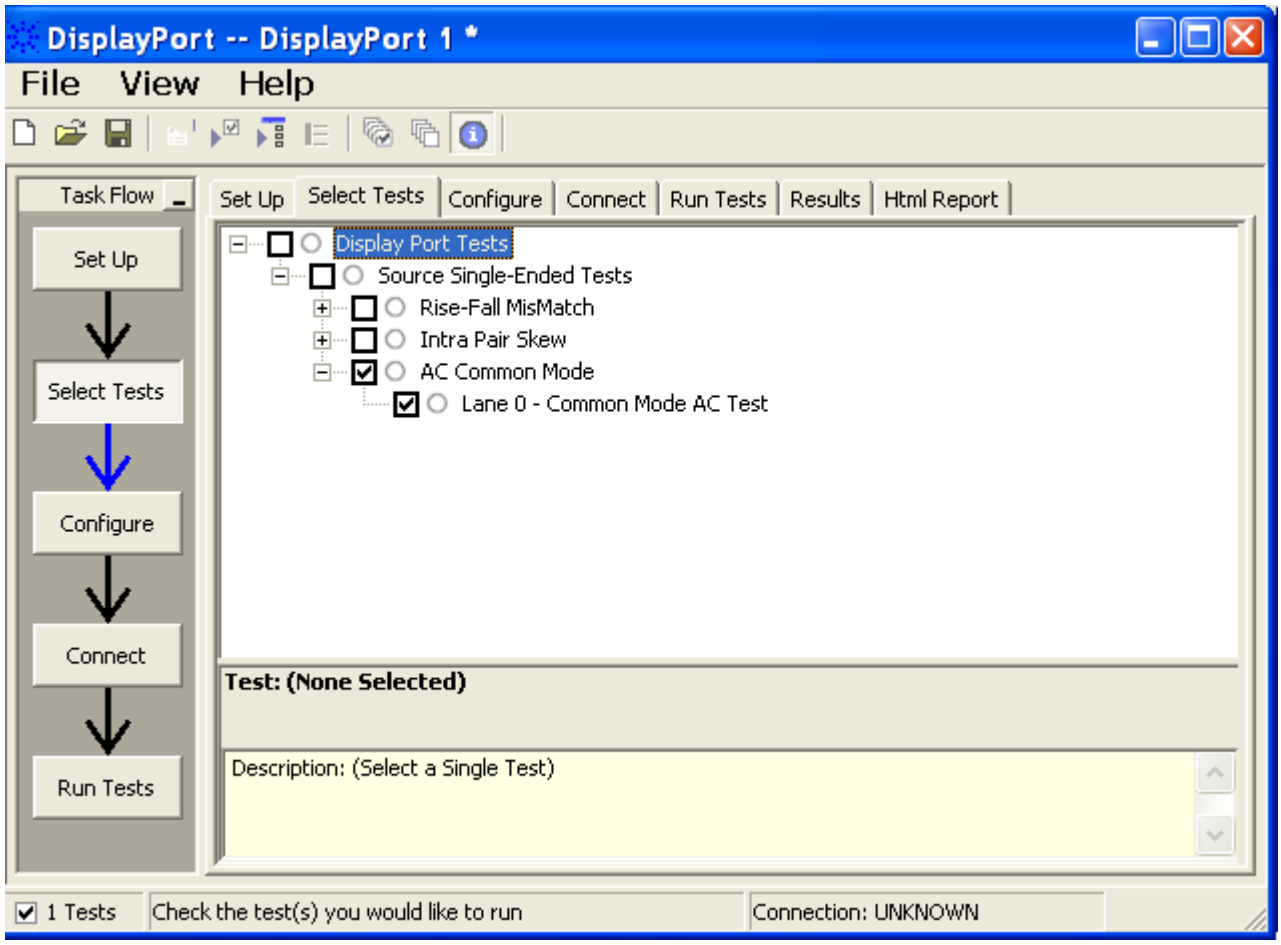

Figure 47 Selecting Transition Time Differential Tests

8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see Table 14), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 14 Test Configuration Options

Configuration Option	Description
Clock Recovery	
Clock Recovery Order	Set either a second order PLL or a first order PLL method is used to recover the clock.
Clock Recovery Loop Bandwidth	Sets the 3 dB bandwidth of the loop filter used by the PLL.
Clock Recovery Damping Factor	Sets the damping factor which is the value that is used in designing the second order PLL that is used to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $$\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$$ where: ω_n = the natural frequency of the PLL ζ = the dampling factor of the PLL F_t = the 3 dB bandwidth of the PLL
Prerequisite Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
PRBS Validation Algorithm Settings	
FFT Memory Length	Sets the memory depth used for FFT calculations.

Table 14 Test Configuration Options

Configuration Option	Description
FFT Acquisition	Sets the number of acquisitions used for FFT calculations.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Interpolation (Debug only)	Specifies whether to turn On or Off the Sin(x)/x interpolation filter. Turning On interpolation may cause more peak-to-peak jitter.
Eye Diagram Mask Movement (Debug only)	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask, (4) Manual mode will allow the user to move the mask manually during the eye test,
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern (Debug only)	Sets the pattern that represents a high or one voltage when three or more ones are transmitted in a row.
Transition VL Pattern (Debug only)	Sets the pattern that represents a low or zero voltage when three or more zeros are transmitted in a row.
Upper Threshold (Debug only)	Sets the upper threshold for the transition tests in percentage.
Lower Threshold (Debug only)	Sets the lower threshold for the transition tests in percentage.
Non-Pre-emphasis	
Level Edges	Sets the number of edges measured for the level test.
Pre-empahsis Level	
Pre-emphasis Edge	Sets the number of edges measured for the level test.
Inter-pair Skew	
Inter-pair Skew Edge	Sets the number of edges measured for the inter-pair skew test.
Maximum Retries	Sets the number of times that the application tries to measure the inter-pair skew test before failing.

Table 14 Test Configuration Options

Configuration Option	Description
Spread Spectrum Clock (SSC)	
SSC Acquisitions	Sets the number of acquisitions taken to verify the SSC.
Single-ended Tests	
Rise-Fall Mismatch	
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Upper Threshold (Debug only)	Sets the upper threshold used to make a rise time or fall time measurement.
Lower Threshold (Debug only)	Sets the lower threshold used to make a rise time or fall time measurement.
Intra-pair Skew	
Intra-pair Edge	Sets the number of edges measured for the intra-pair skew test.
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.

PASS Condition

AC Common Mode Noise = Nominal Frequency ±300 ppm.

Test References

See Test 3.10: AC Common Mode Noise, in the *DisplayPort- Compliance Test Specification Version 1.*

14
Calibrating the Infiniium Oscilloscope and Probe

This chapter describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DisplayPort automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the Agilent Infiniium oscilloscopes).
- E2655A/B probe de-skew fixture.
- 82 Ω damping resistors (01130-81506) for the Socketed Differential Probe Head.

Figure 48 below shows a drawing of the above connector items.

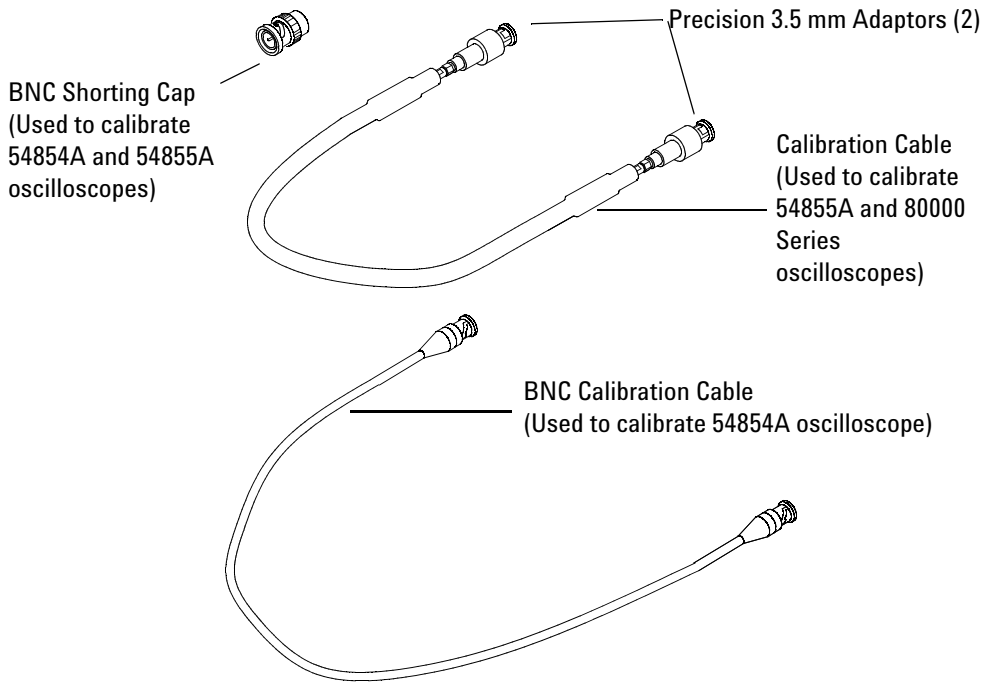

Figure 48 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b If a second monitor is being used, connect it to the VGA connector located near the LAN port, on the rear of the oscilloscope.

   c Plug in the power cord.

   d Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   e Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 2 below.

2 Locate and prepare the accessories that will be required for the internal calibration

   f Locate the calibration cable.

   g Locate the two Agilent precision SMA/BNC adapters.

   h Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   i Attach the other SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 49 below, perform the following steps:

a Click on the **Utilities>Calibration** menu to open the Calibration window.

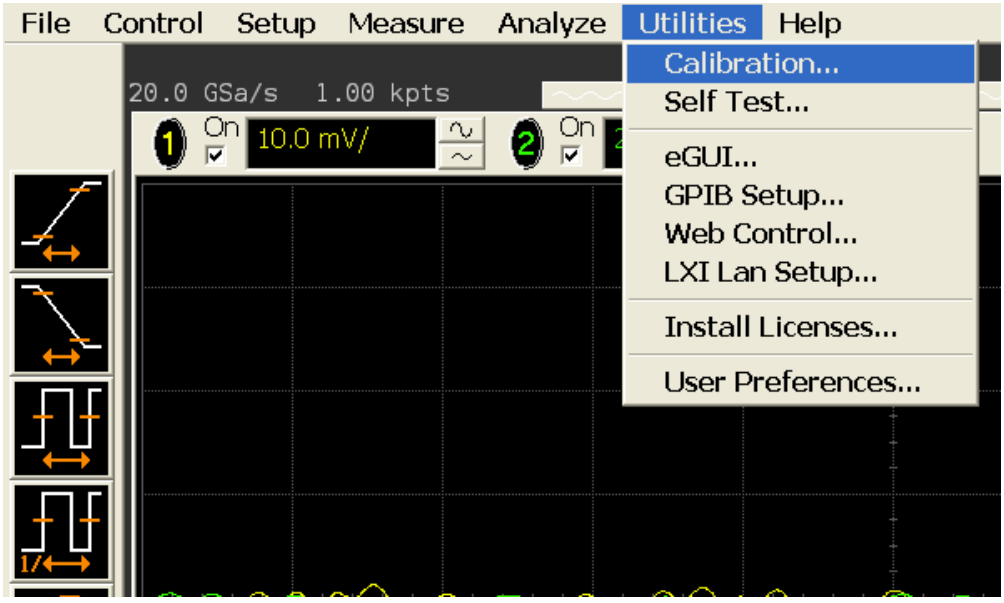

Figure 49 Accessing the Calibration Menu.

4 Referring to Figure 50 below, perform the following steps to start the calibration:

a Uncheck the Cal Memory Protect checkbox.

b Click the Start button to begin the calibration.

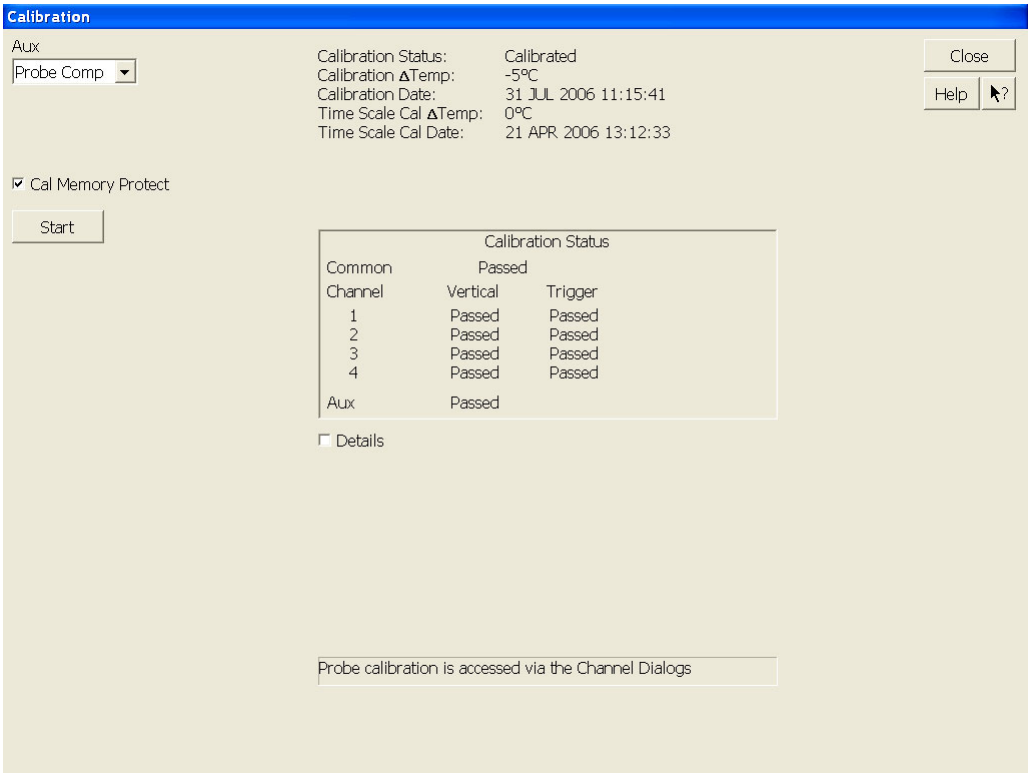

Figure 50 Oscilloscope Calibration Window

5 Follow the on-screen instructions:

a You will be prompted to disconnect everything from all the inputs: click the OK button.

b Then you will be prompted to connect the calibration cable with SMA adapters between the Aux Out and a specified input. Install the SMA adapter by pressing it on input BNC, and hand tightening the outer ring turning right. Click the OK button after connecting the cable as prompted.

c During the calibration of channel 1, you will be prompted a Calibration Options screen, as shown in Figure 51 below.

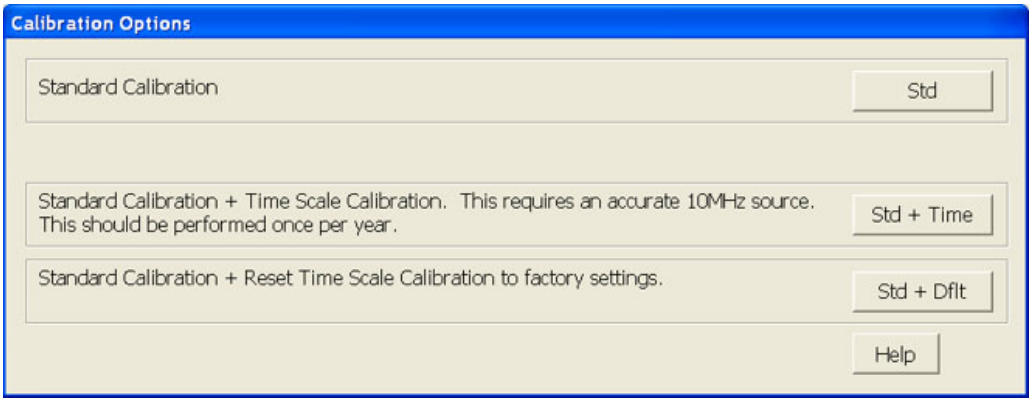

Figure 51 Time Scale Calibration Dialog box

d Click on the Std + Dflt button to continue the calibration, using the Factory default calibration factors.

e When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

f Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

g Click the Close button to close the calibration window.

h The internal calibration is completed.

i Read NOTE below.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Probe Calibration and De-skew

Before performing DisplayPort tests you should calibrate and de-skew the probes.

SMA probe head Atten/Offset Calibration

1 Referring to Figure 52 below, perform the following steps:

a Ensure that a probe, attached with SMA probe head is connected to Channel 1. Install the 82 Ω resistors into the SMA probe head. Connect the de-skew fixture to Aux Out. Clip the resistors on de-skew fixture. These resistors are only required for probe calibration and de-skew.

b Click on the **Setup>Channel 1** menu to open the Channel Setup window.

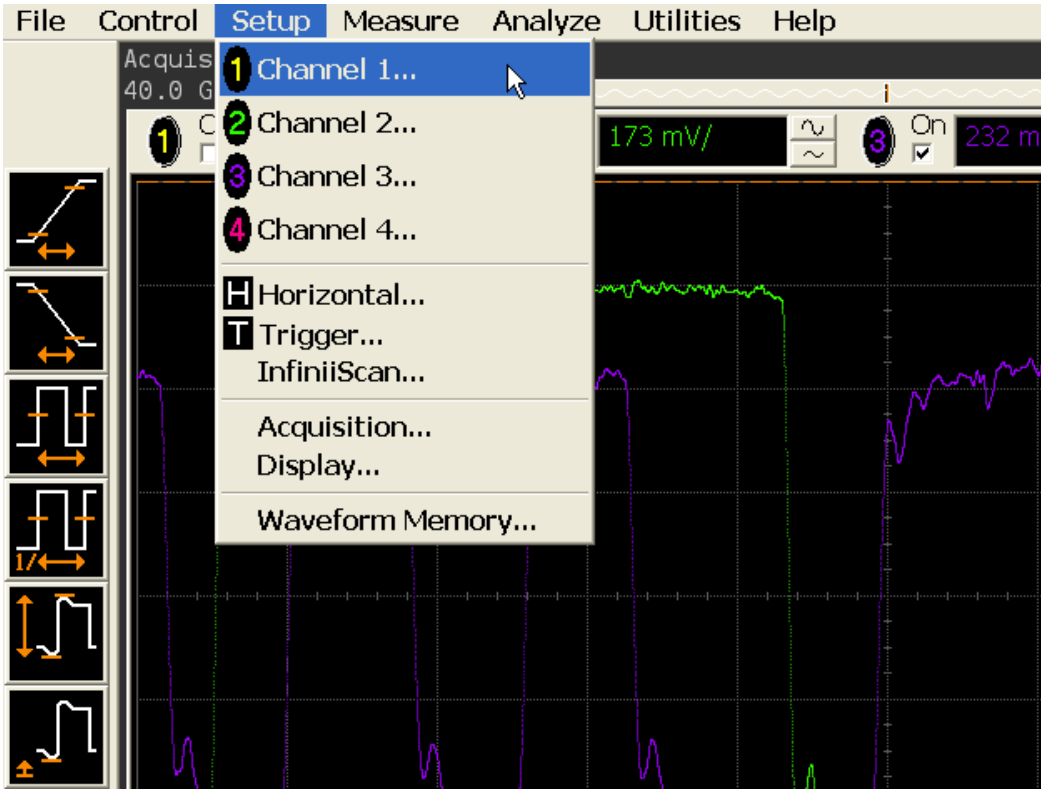

Figure 52 Channel Setup Window.

c Click the Probes button in the Channel Setup window, to open the Probe Setup window.

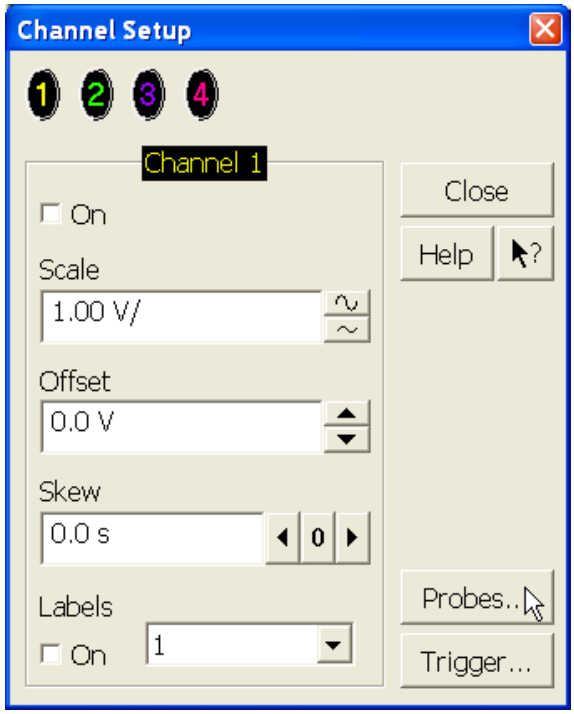

Figure 53 Channel Dialog Box

2 Referring to Figure 54 below, perform the following steps:

a Click the Add Head... button, and then select E2678A:DF Sckt from the list of Head Type. Select OK to close the dialog box.

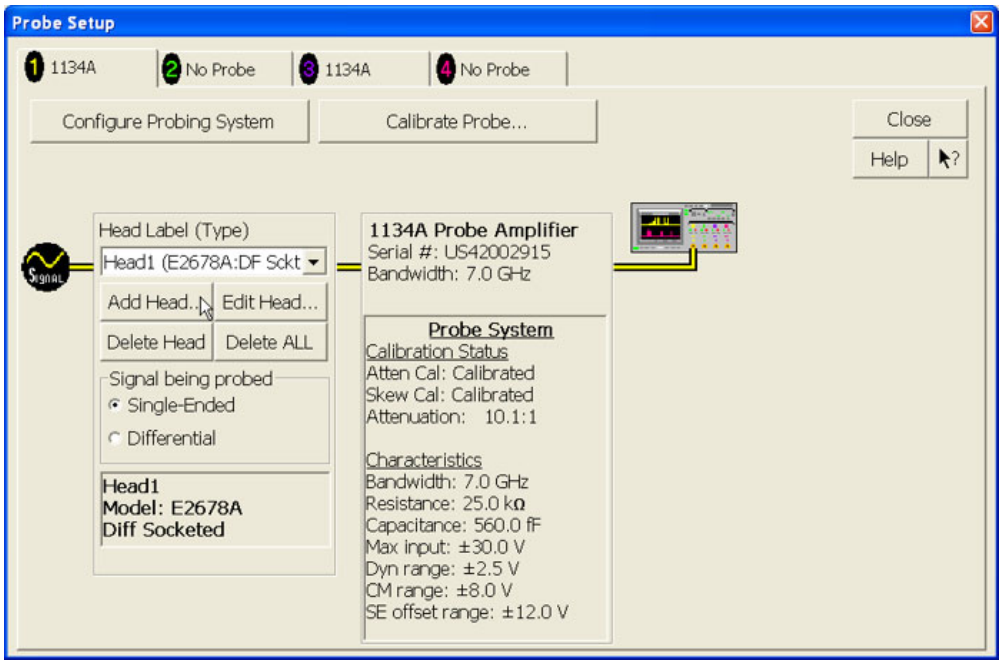

Figure 54 Probe Setup Window.

3 Referring to Figure 55 below, perform the following steps:

a Click on the Calibrate Probe button to open the Probe Calibration window.

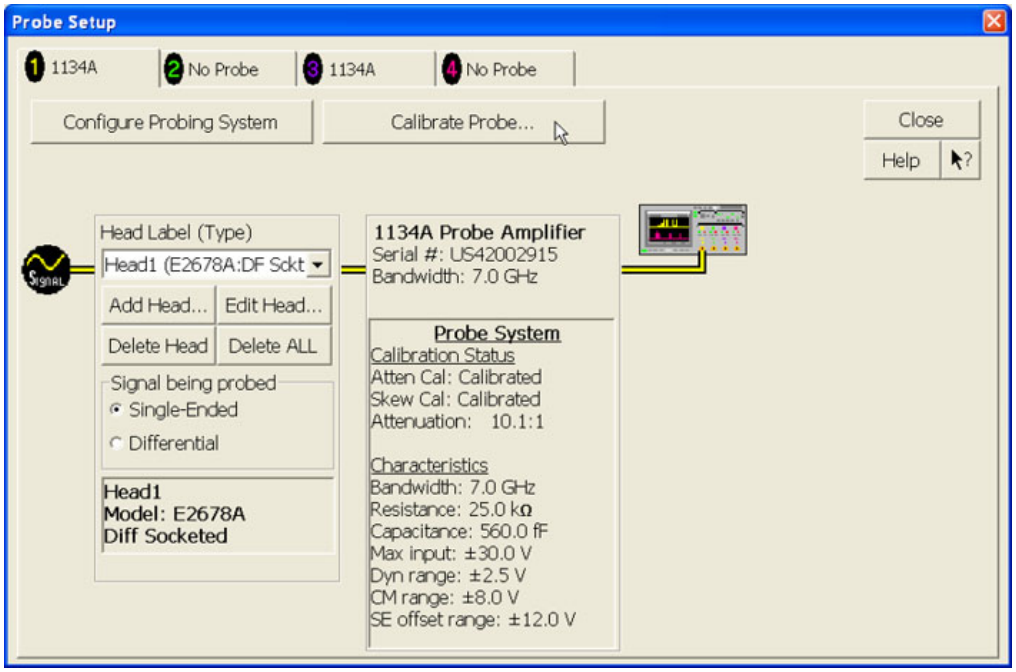

Figure 55 User Defined Probe Window.

4 Referring to Figure 56 and perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

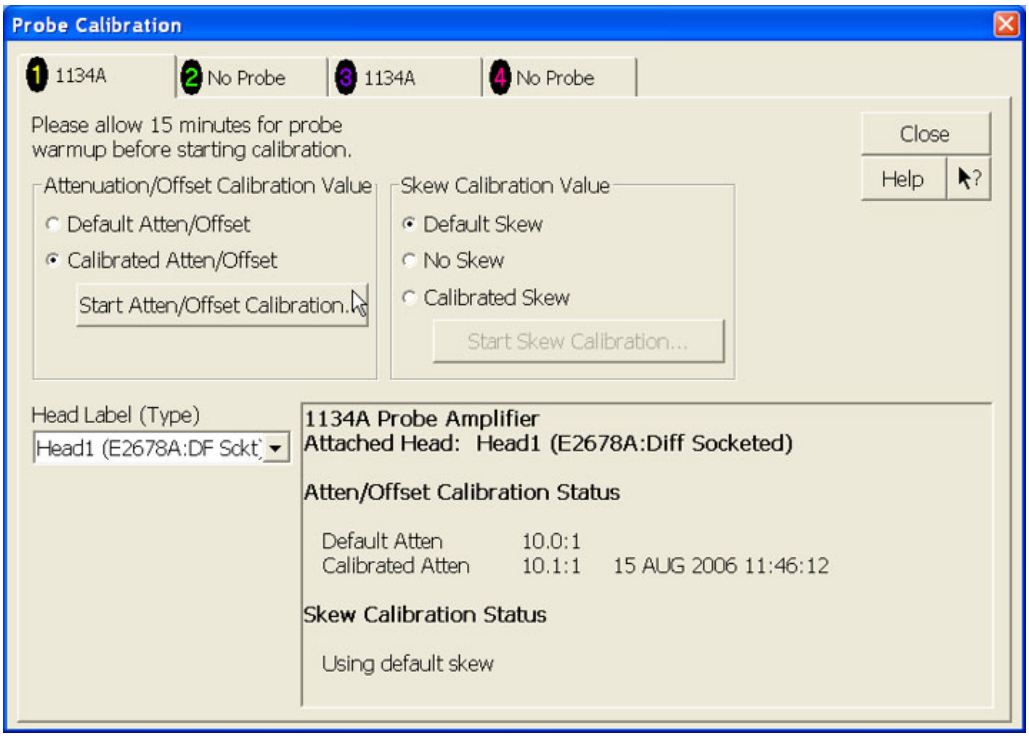

Figure 56 Probe Calibration Window.

c Follow the on-screen instructions.

d At the end of the Atten/Offset Calibration perform the Skew Calibration.

Differential Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. Perform the following steps:

1 Referring to Figure 57 below, perform the following steps:

a Select the Start Skew Calibration button and follow the on-screen instructions. For more information on proper connection of probe to the oscilloscope, refer to the De-skew and Calibration manual. This

manual comes together with the E2655A/B De-skew Kit, that came with your oscilloscope.

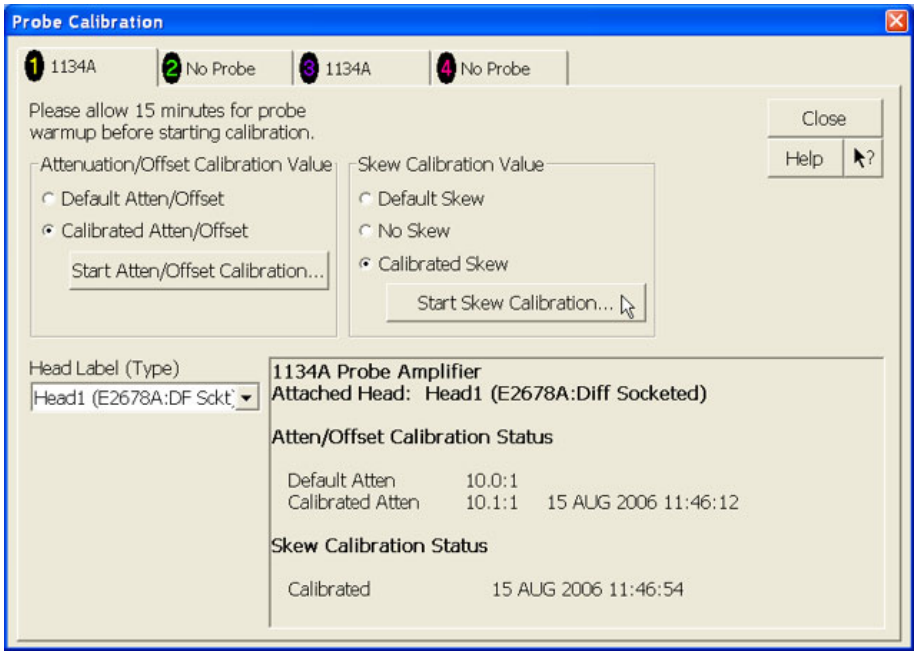

Figure 57 De-skew Connection.

NOTE Each probe is calibrated to the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes are labeled with the channel on which they were calibrated.

SMA Probe Head Atten/Offset Calibration

1 Referring to Figure 58 below, perform the following steps:

- **a** Connect the SMA to BNC adaptor to one of the SMA connectors of the deskew fixture or SMA (f) to SMA (f) adapter.
- **b** Connect the 50 ohm terminator to the center SMA connector of the SMA probe head.
- **c** Connect the other end of the deskew fixture or SMA (f) to SMA (f) adapter to one of the SMA connectors of the SMA probe head.
- **d** Connect the BNC connector of the SMA to BNC adaptor to the Aux Out on the front panel of the Infiniium oscilloscope.
- **e** Connect the positive (+) side of the InfiniiMax probe amp to the GPO (SMP) connector of the SMA probe head whose path is connected to

the Aux Out of the oscilloscope. Do not connect the negative (-) side of the InfiniiMax probe amp to anything.

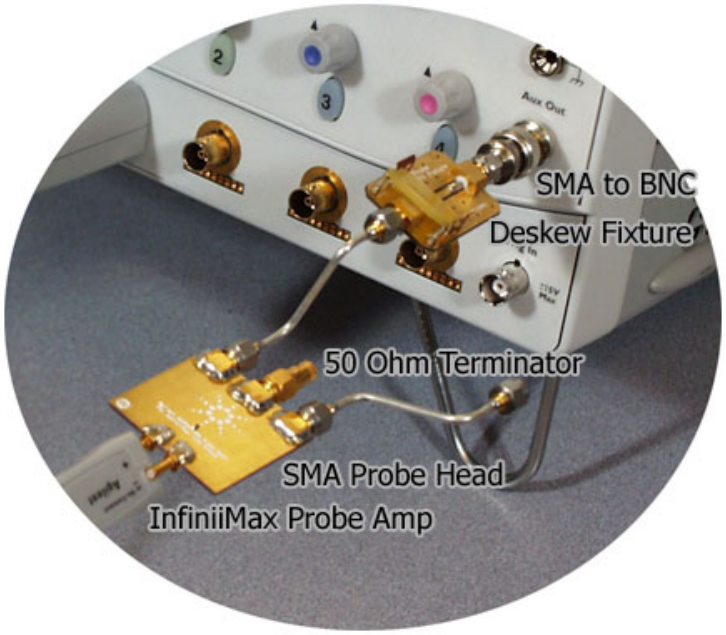

Figure 58 SMA Probe Head Calibration

f Click on the **Setup>Channel 1** menu to open the Channel Setup window.

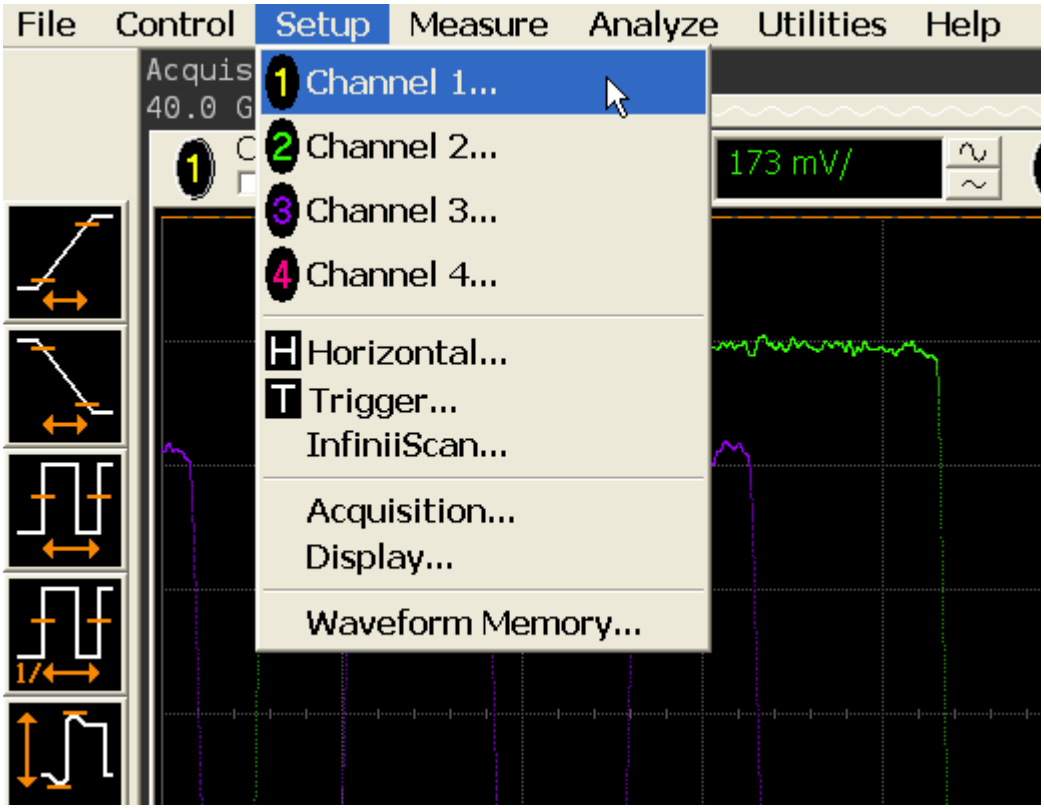

Figure 59 Channel Setup Window

g Click the Probes button in the Channel Setup window, to open the Probe Setup window.

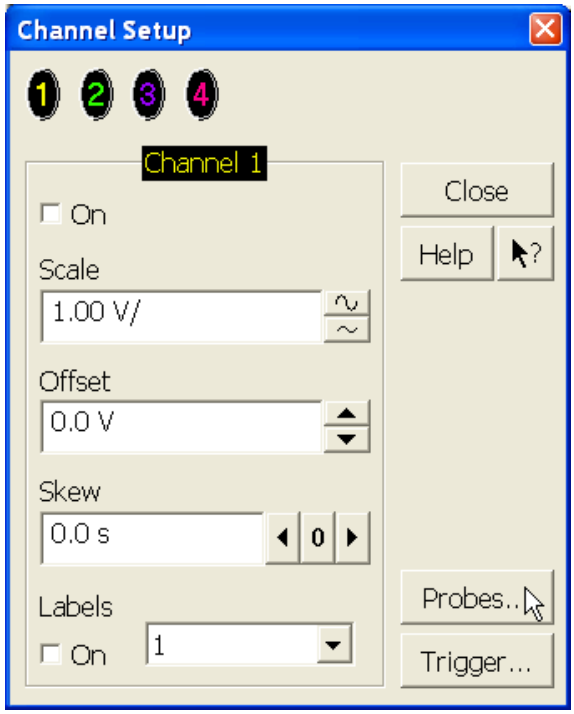

Figure 60 Channel Dialog Box

2 Referring to Figure 61 below, perform the following steps:

a Click the Add Head... button, and then select N5380A:DF SMA from the list of Head Type. Select OK to close the dialog box.

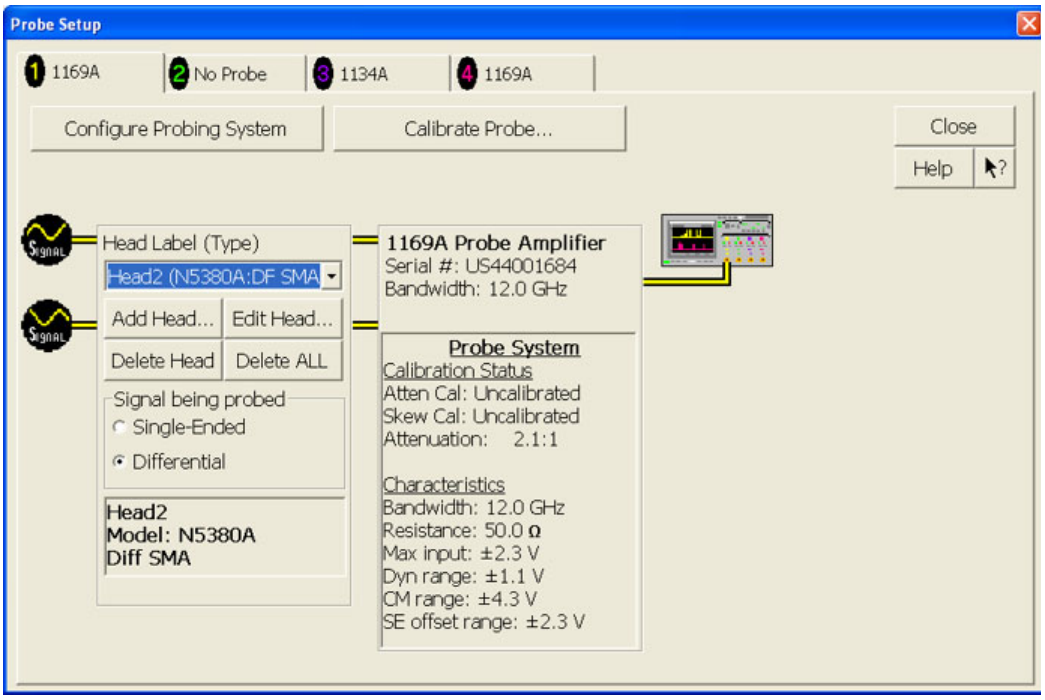

Figure 61 Probe Setup Window.

b Click on the Calibrate Probe button to open the Probe Calibration window.

3 Referring to Figure 62 below, perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

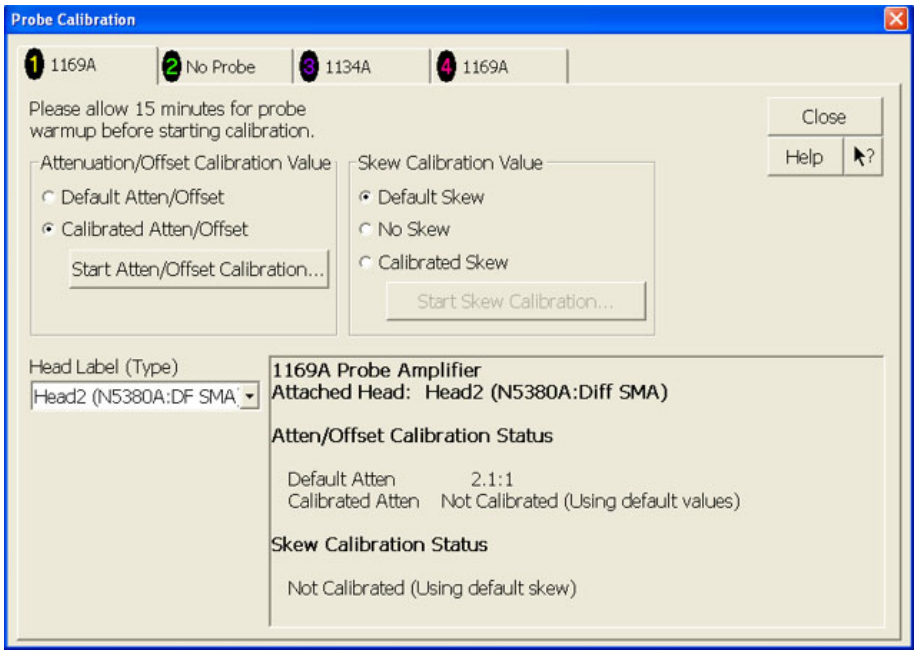

Figure 62 Probe Calibration Window.

c Follow the on-screen instructions.

d At the end of the Atten/Offset Calibration perform the Skew Calibration.

SMA Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. Perform the following steps:

1 Referring to Figure 63 below, perform the following steps:

a Select the Start Skew Calibration button and follow the on-screen instructions. For more information on proper connection of probe to the oscilloscope, refer to the De-skew and Calibration manual. This

manual comes together with the E2655A/B De-skew Kit, that came with your oscilloscope.

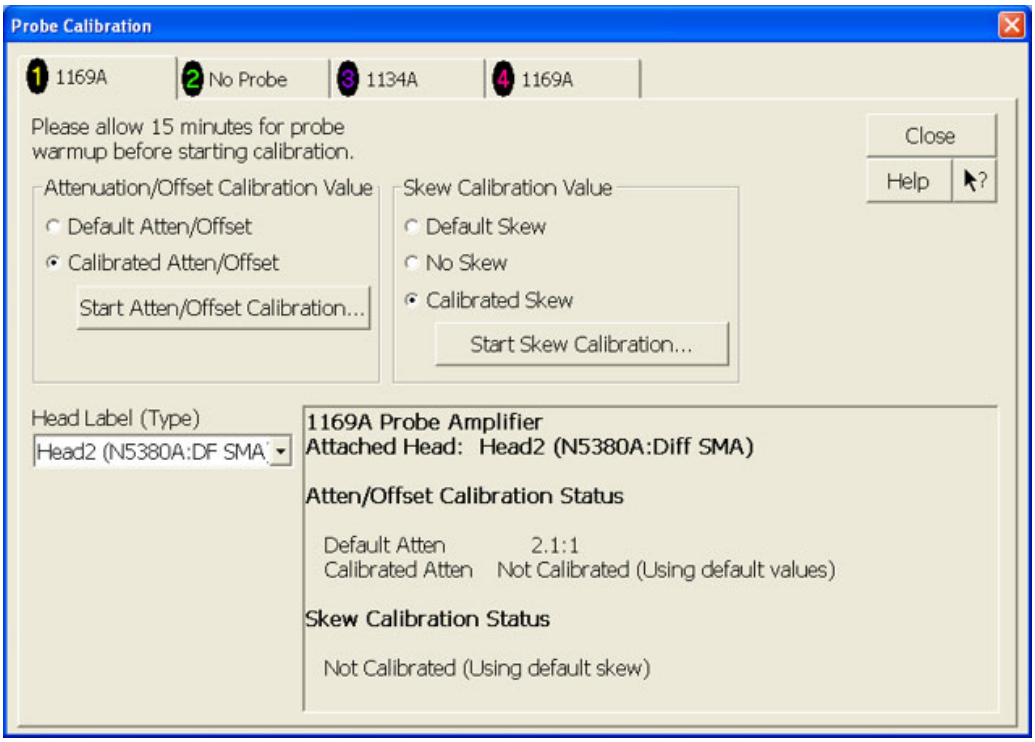

Figure 63 De-skew Connection.

15 InfiniiMax Probing

Figure 64 1169A InfiniiMax Probe Amplifier

Agilent recommends the N5380A SMA probe head and the N5380A differential SMA probe head.

Figure 65 Recommended Socketed Probe Head for the DisplayPort Testing

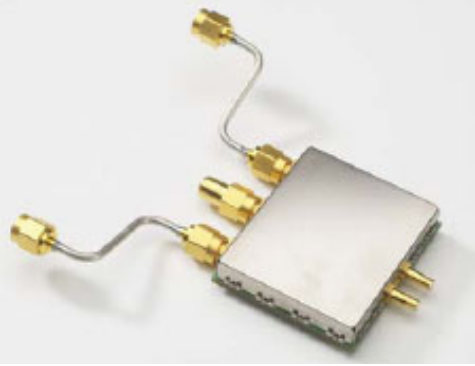

Figure 66 Recommended SMA Probe Head for DisplayPort Testing

Table 15 Probe Head Characteristics

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential socket	E2678A	7 GHz, 0.34 pF, 50 kOhm	7 GHz, 0.56 pF, 25 kOhm
Hi-BW differential SMA	N5380A	12 GHz	12 GHz

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First edition, July 2007
This part is not orderable.

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